Flash 1 Gbit (128M x 8/ 64M x 16) 1.8V NAND Flash Memory

FEATURES

- Voltage Supply: 1.8V (1.7 V ~ 1.95V)
- Organization
  x8:
  - Memory Cell Array: (128M + 4M) x 8bit
  - Data Register: (2K + 64) x 8bit
  x16:
  - Memory Cell Array: (64M + 2M) x 16bit
  - Data Register: (1K + 32) x 16bit
- Automatic Program and Erase
  x8:
  - Page Program: (2K + 64) Byte
  - Block Erase: (128K + 4K) Byte
  x16:
  - Page Program: (1K + 32) Word
  - Block Erase: (64K + 2K) Word
- Page Read Operation
  x8
  - Page Size: (2K + 64) Byte (x8)
  - Random Read: 25us (Max.)
  - Serial Access: 45ns (Min.)
  x16
  -Page Size: (1K + 32) Word (x16)
- Memory Cell: 1bit/Memory Cell
- Fast Write Cycle Time
  x8
  - Program time: 300us (Typ.)
  - Block Erase time: 4ms (Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - ECC Requirement: x8 - 4bit/512Byte,
    x16 - 4bit/256Word
  - Endurance: 100K Program/Erase Cycles
  - Data Retention: 10 Years
- Command Register Operation
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download
- NOP: 4 cycles
- Cache Program/Read Operation for High Performance Program
- Cache Read Operation
- Copy-Back Operation
- EDO mode
- Bad-Block-Protect
- One Time Program (OTP) Operation

ORDERING INFORMATION

Product ID	Speed	Package	Comments
x8:			
F59D1G81MB-45TIG2M	45 ns	48 pin TSOPI	Pb-free
F59D1G81MB-45BUIG2M	45 ns	48 ball BGA	Pb-free
F59D1G81MB-45BIG2M	45 ns	63 ball BGA	Pb-free
F59D1G81MB-45BCIG2M	45 ns	67 ball BGA	Pb-free
x16:			
F59D1G161MB-45TIG2M	45 ns	48 pin TSOPI	Pb-free
F59D1G161MB-45BIG2M	45 ns	63 ball BGA	Pb-free

GENERAL DESCRIPTION

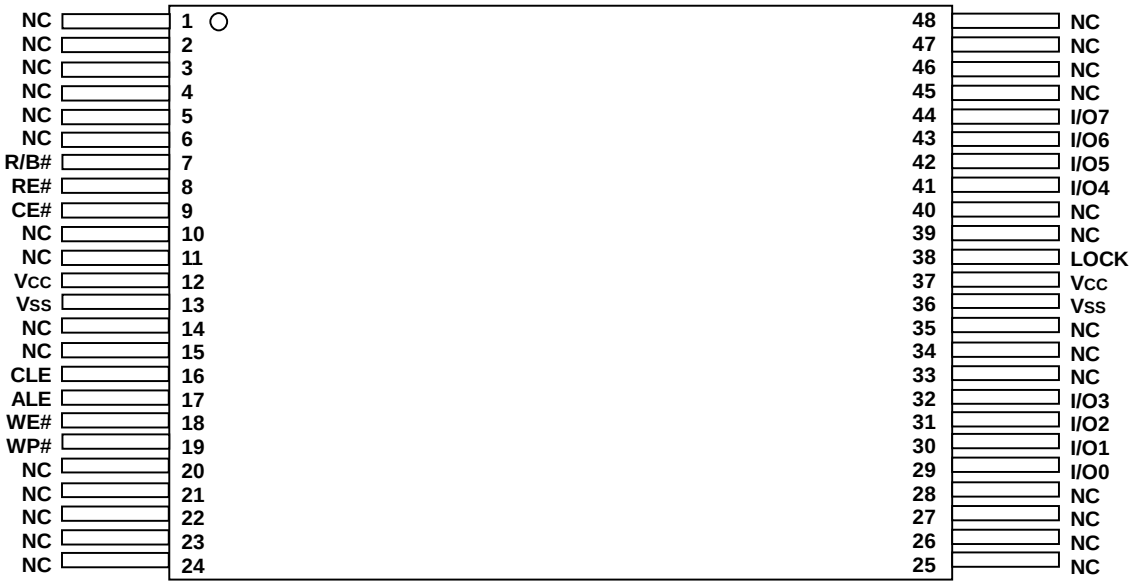
The Device is a 128Mx8bit with spare 4Mx8bit capacity. The device is offered in 1.8V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 2,112-Byte page in typical 300us and an erase operation can be performed in typical 4ms on a 128K-Byte for X8 device block.

Data in the page mode can be read out at 45ns cycle time per Byte. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

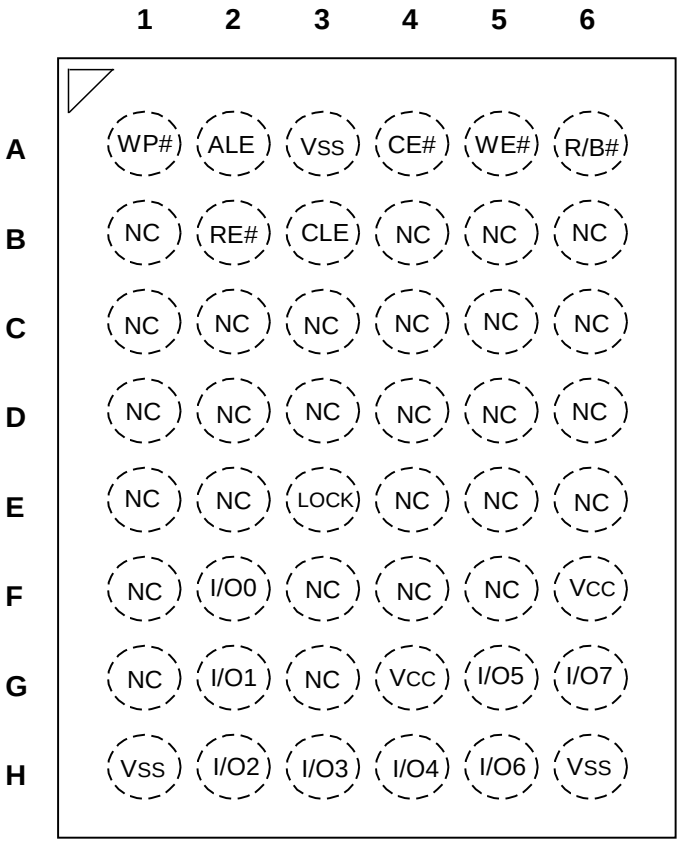
PIN CONFIGURATION (x8) (TOP VIEW)

(TSOPI 48L, 12mm X 20mm Body, 0.5mm Pin Pitch)



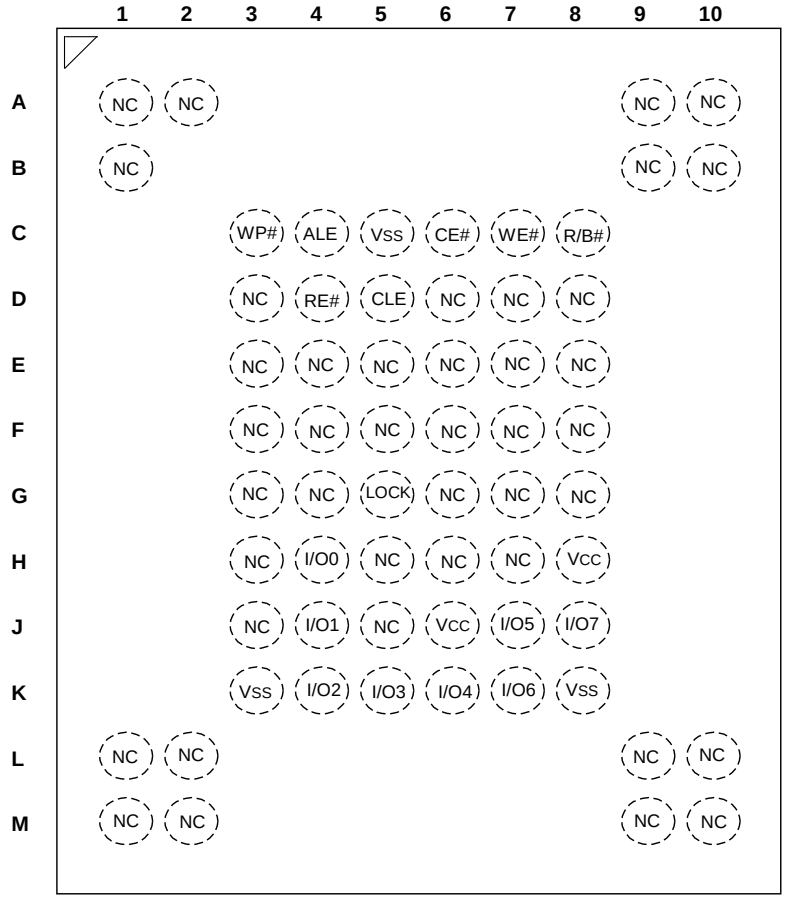
BALL CONFIGURATION (x8) (TOP VIEW)

(BGA 48 BALL, 6.5mm X 5mm Body, 0.8 Ball Pitch)



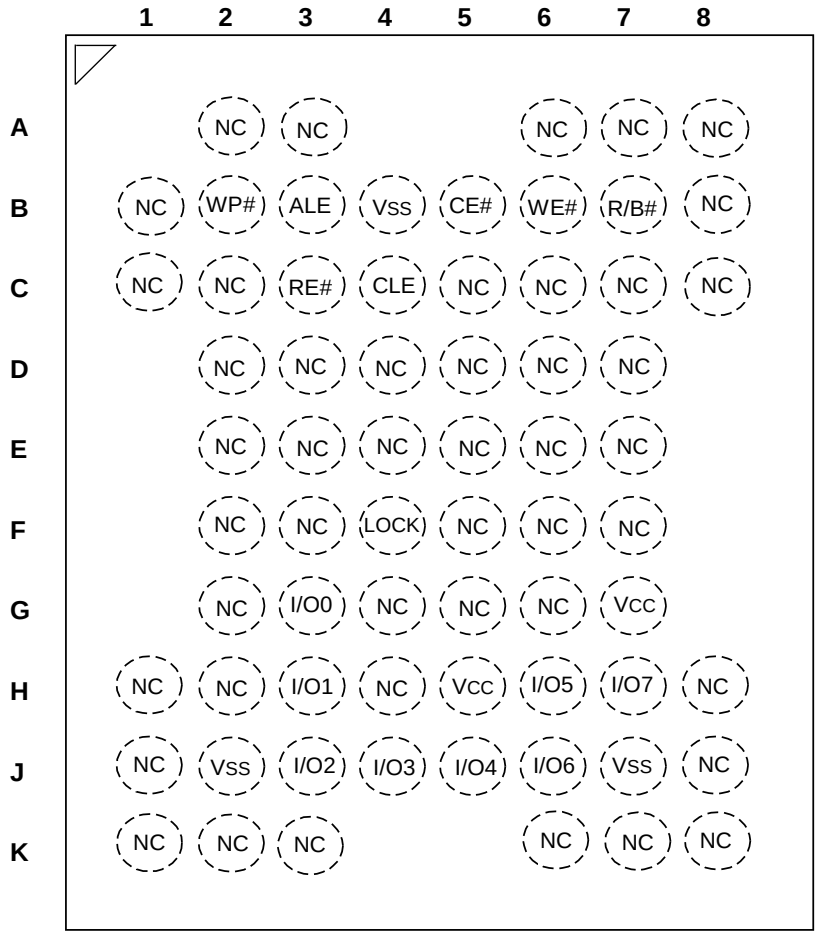
BALL CONFIGURATION (x8) (TOP VIEW)

(BGA 63 BALL, 9mm X 11mm Body, 0.8 Ball Pitch)



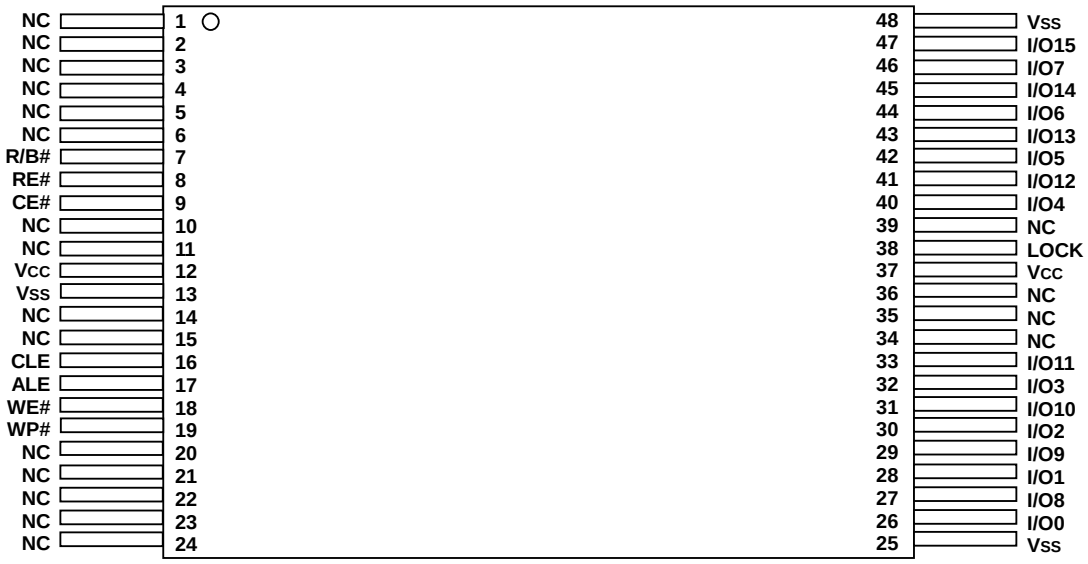
BALL CONFIGURATION (x8) (TOP VIEW)

(BGA 67 Ball, 6.5mmx8mmx1.0mm Body, 0.8mm Ball Pitch)



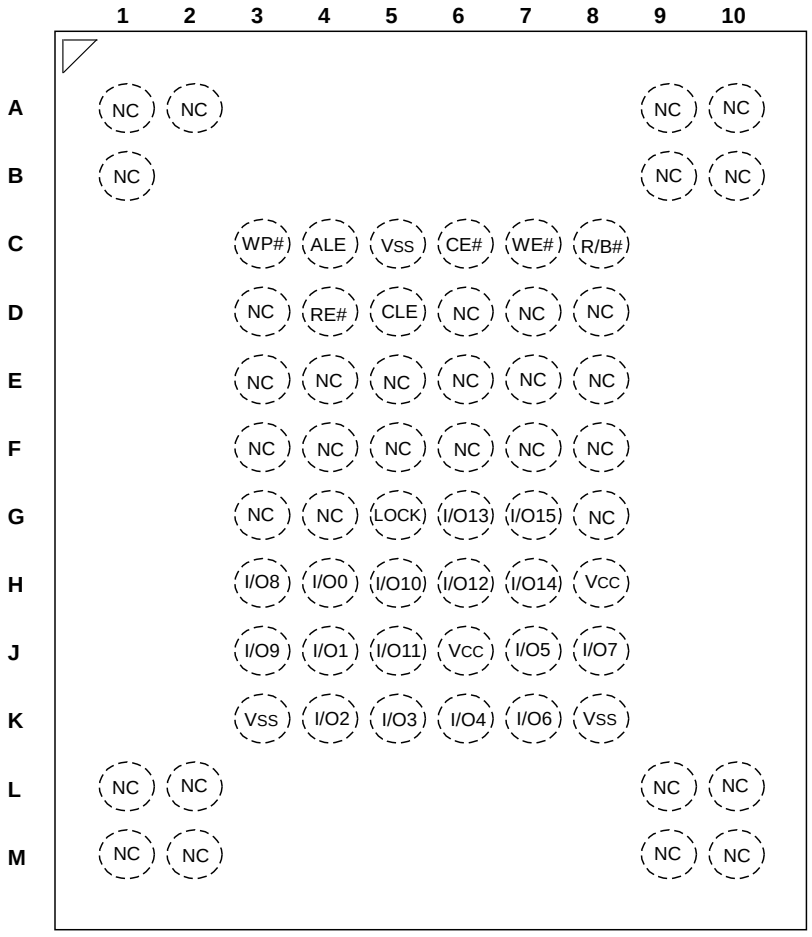
PIN CONFIGURATION (x16) (TOP VIEW)

(TSOPI 48L, 12mm X 20mm Body, 0.5mm Pin Pitch)



BALL CONFIGURATION (x16) (TOP VIEW)

(BGA 63 BALL, 9mm X 11mm Body, 0.8 Ball Pitch)

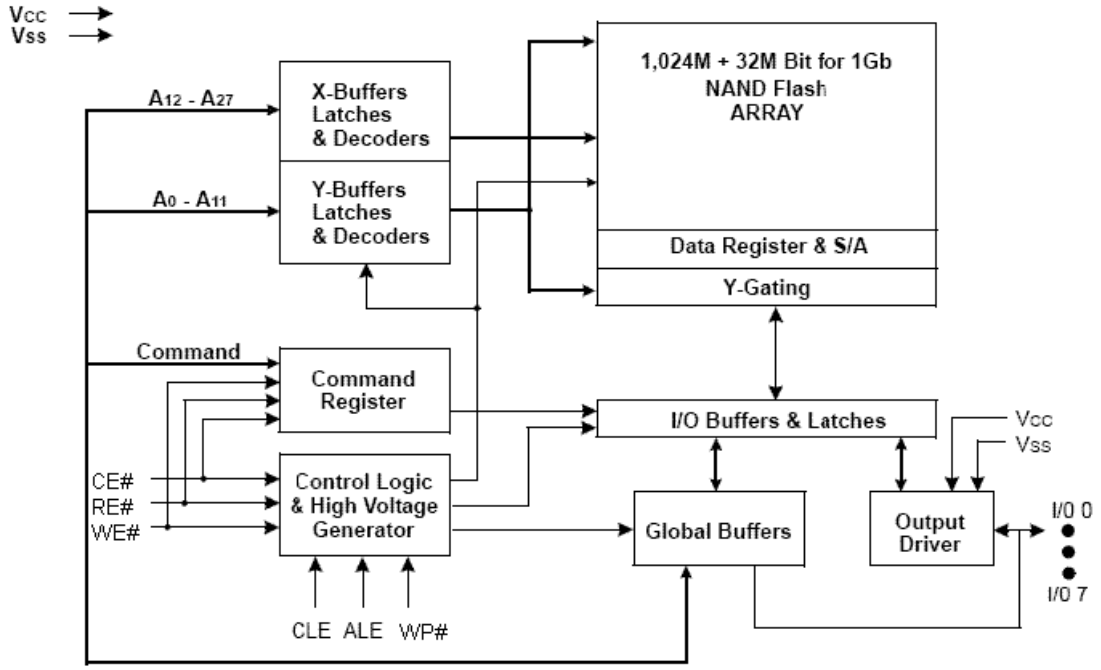


Pin Description

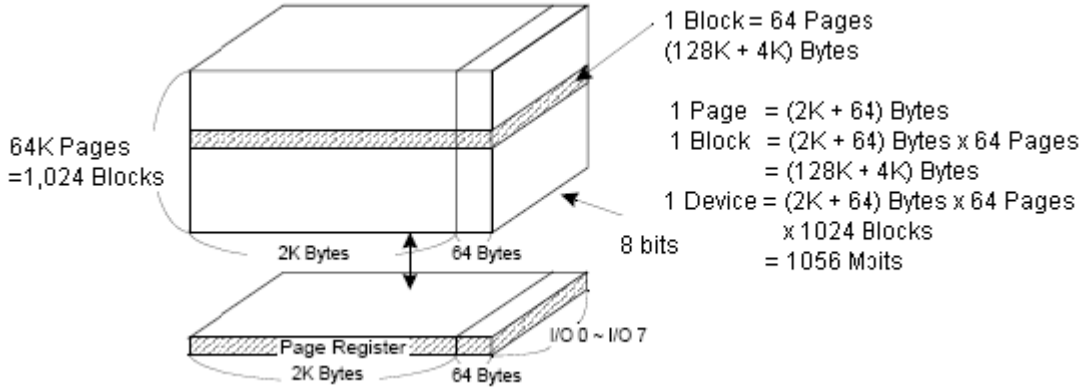
Symbol	Pin Name	Functions
I/O0~I/O7 (x8) I/O0~I/O15 (x16)	Data Inputs / Outputs	The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	Command Latch Enable	The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	Address Latch Enable	The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	Chip Enable	The RE# input is the device selection control. When the device is in the Busy state, RE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
LOCK	LOCK	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to VSS during power-up, or leave it unconnected (internal pull-doyn).
RE#	Read Enable	The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	Write Enable	The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	Write Protect	TheWP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	Ready / Busy Output	The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{CC}	Power	V_{CC} is the power supply for device.
V_{SS}	Ground	
NC	No Connection	Lead is not internally connected.

Note: Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

BLOCK DIAGRAM (x8)



ARRAY ORGANIZATION (x8)

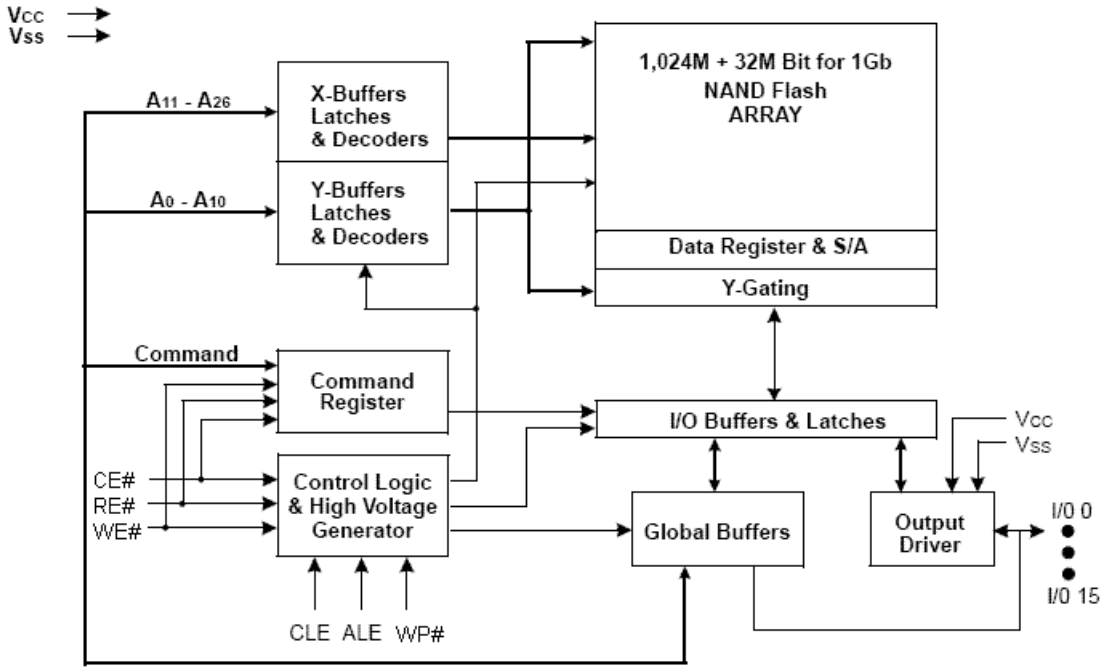


Address Cycle Map (x8)

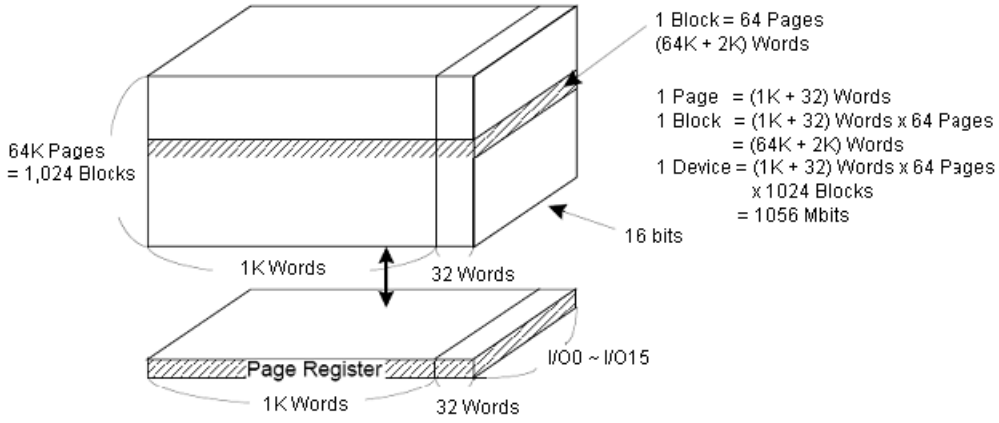
	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	Address
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd cycle	A8	A9	A10	A11	*L	*L	*L	*L	**Column Address**
3rd cycle	A12	A13	A14	A15	A16	A17	A18	A19	**Row Address**
4th cycle	A20	A21	A22	A23	A24	A25	A26	A27	**Row Address**

NOTE:
Column Address: Starting Address of the Register.
* L must be set to "Low".
* The device ignores any additional input of address cycles than required.
* A12~A17 are for Page Address, A18~A27 are for Block Address.

BLOCK DIAGRAM (x16)



ARRAY ORGANIZATION (x16)



Address Cycle Map (x16)

	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8~I/O15	Address
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7	*L	**Column Address**
2nd cycle	A8	A9	A10	*L	*L	*L	*L	*L	*L	**Column Address**
3rd cycle	A11	A12	A13	A14	A15	A16	A17	A18	*L	**Row Address**
4th cycle	A19	A20	A21	A22	A23	A24	A25	A26	*L	**Row Address**

NOTE:
Column Address: Starting Address of the Register.
* L must be set to “Low”.
* The device ignores any additional input of address cycles than required.
* A11~A16 are for Page Address, A17~A26 are for Block Address

Product Introduction

The device is a 1,056Mbit memory organized as 128K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1,024 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the device.

The device has addresses multiplexed into 8 I/Os or 16I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

Command Set

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	**O**
BLOCK UNLOCK LOW / HIGH	23h	24h	
BLOCK LOCK	2Ah		
BLOCK LOCK-TIGHT	2Ch		
BLOCK LOCK READ STATUS	7Ah		O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Read Status	70h	-	**O**
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Read Parameter Page	ECh	-	
Read Unique ID	EDh	-	

NOTE: Random Data Input / Output can be executed in a page.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +2.45	V
	V_{IN}	-0.6 to +2.45	
	$V_{I/O}$	-0.6 to V_{CC} + 0.3 (< 2.45V)	
Temperature Under Bias	T_{BIAS}	-40 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Short Circuit Current	I_{OS}	5	mA

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A = -40~85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	t_{RC}=45ns, CE#=V_{IL}, I_{OUT}=0mA	-	15	20	mA
	Program	I_{CC2}	-	-	15		
	Erase	I_{CC3}	-	-	15		
Stand-by Current (TTL)		I_{SB1}	CE#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CE#= V_{CC} -0.2, WP#=0V/ V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH}(1)	-	0.8 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL}(1)	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-100uA	V_{CC} - 0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=+100uA	-	-	0.1	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/B#)	V_{OL}=0.2V	3	4	-	mA

NOTE:
1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC}+0.4V for durations of 20ns or less.
2. Typical value are measured at V_{CC} =1.8V, T_A=25℃. And not 100% tested.

VALID BLOCK

Parameter	Symbol	Min.	Typ.	Max.	Unit
F59D1G81MB/ F59D1G161MB	N_{VB}	1,004	-	1,024	Blocks

NOTE:
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 4bit/512Byte ECC.

AC TEST CONDITION

(T_A= -40~85℃, V_{CC}=1.7V~1.95V)

Parameter	Condition
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=30pF

NOTE:
Refer to 11.10 Ready/Busy#, R/B# output's Busy to Ready time is decided by the pull-up resistor (Rp) tied to the R/B# pin.

CAPACITANCE

(T_A=25℃, V_{CC}=1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (4 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (4 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE:
1. X can be V_{IL} or V_{IH}.
2. WP# should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

(T_A= -40~85℃, Vcc=1.7V ~ 1.95V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Average Program Time	t_{PROG}	-	350	750	us
Dummy Busy Time for Cache Operation	t_{CBSY}	-	3	750	us
Last Page Program Time	t_{LPROG}	-	-	900	us
Number of Partial Program Cycles in the Same Page	N_{OP}	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	4	10	ms
Busy Time for Program / Erase on Locked Blocks	t_{LBSY}	-	-	3	us

NOTE:
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V V_{CC} and 25℃ temperature.
2. t_{PROG} is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.
3. t_{LPROG} = t_{PROG} (last page) + t_{PROG} (last-1 page) – Command load time (last page) – Address load time (last page) – Data load time (last page).

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min.	Max.	Unit
CLE Setup Time	t_{CLS}(1)	25	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
CE# Setup Time	t_{CS}(1)	35	-	ns
CE# Hold Time	t_{CH}	10	-	ns
WE# Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}(1)	25	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}(1)	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
WE# High Hold Time	t_{WH}	15	-	ns
Address to Data Loading Time	t_{ADL}(2)	100	-	ns

NOTE:
1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

AC Characteristics for Operation

Parameter		Symbol	Min.	Max.	Unit
Data Transfer from Cell to Register		t_R	-	25	us
ALE to RE# Delay		t_{AR}	10	-	ns
CLE to RE# Delay		t_{CLR}	10	-	ns
Ready to RE# Low		t_{RR}	20	-	ns
RE# Pulse Width		t_{RP}	25	-	ns
WE# High to Busy		t_{WB}	-	100	ns
WP# Low to WE# Low (disable mode)		t_{WW}	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		t_{RC}	45	-	ns
RE# Access Time		t_{REA}	-	30	ns
CE# Access Time		t_{CEA}	-	45	ns
RE# High to Output Hi-Z		t_{RHZ}	-	100	ns
CE# High to Output Hi-Z		t_{CHZ}	-	30	ns
CE# High to ALE or CLE Don't care		t_{CSD}	0	-	ns
RE# High to Output Hold		t_{RHOH}	15	-	ns
RE# Low to Output Hold		t_{RLOH}	5	-	ns
CE# High to Output Hold		t_{COH}	15	-	ns
RE# High Hold Time		t_{REH}	15	-	ns
Output Hi-Z to RE# Low		t_{IR}	0	-	ns
RE# High to WE# Low		t_{RHW}	100	-	ns
WE# High to RE# Low		t_{WHR}	60	-	ns
Device Resetting Time during ...	Read	t_{RST}	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5(1)	us
Cache Busy in Read Cache (following 31h and 3Fh)		t_{DCBSYR}	-	30	us

NOTE: If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

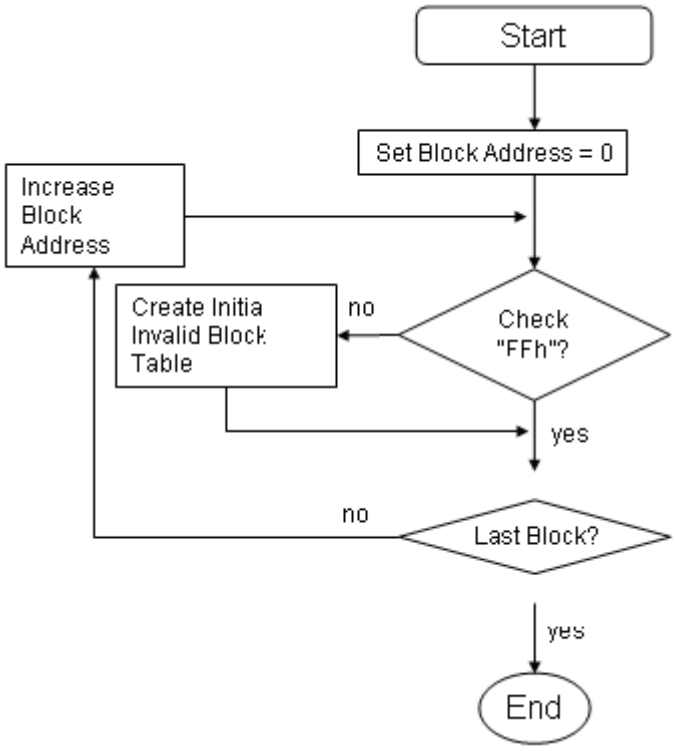
Mask Out Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ESMT. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 4bit/512Byte ECC.

Identifying Initial Invalid Block(s) and Block Replacement Management

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. ESMT makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the 1st byte column address in the spare area. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart. Any intentional erasure of the initial invalid block information is prohibited.

Algorithm for Bad Block Scanning



Check “FFh” at column address 2048 of the first page and the second page

```
For (i=0; i<Num_of_LUs; i++)
{
      For (j=0; j<Blocks_Per_LU; j++)
      {
            Defect_Block_Found=False;

            Read_Page(lu=i, block=j, page=0);
            If (Data[coloumn= First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

            Read_Page(lu=i, block=j, page=1);
            If (Data[coloumn= First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

            If (Defect_Block_Found)        Mark_Block_as_Defective(lu=i, block=j);
       }
}
```

Figure Algorithm for Bad Block Scanning

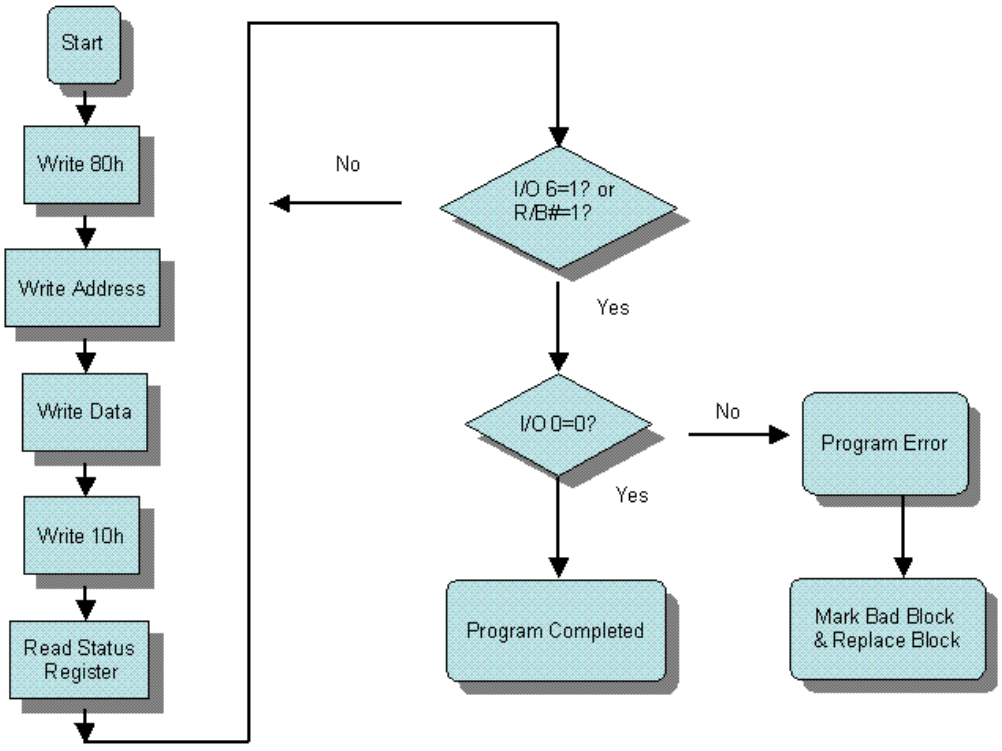
Error in Write or Read operation

Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

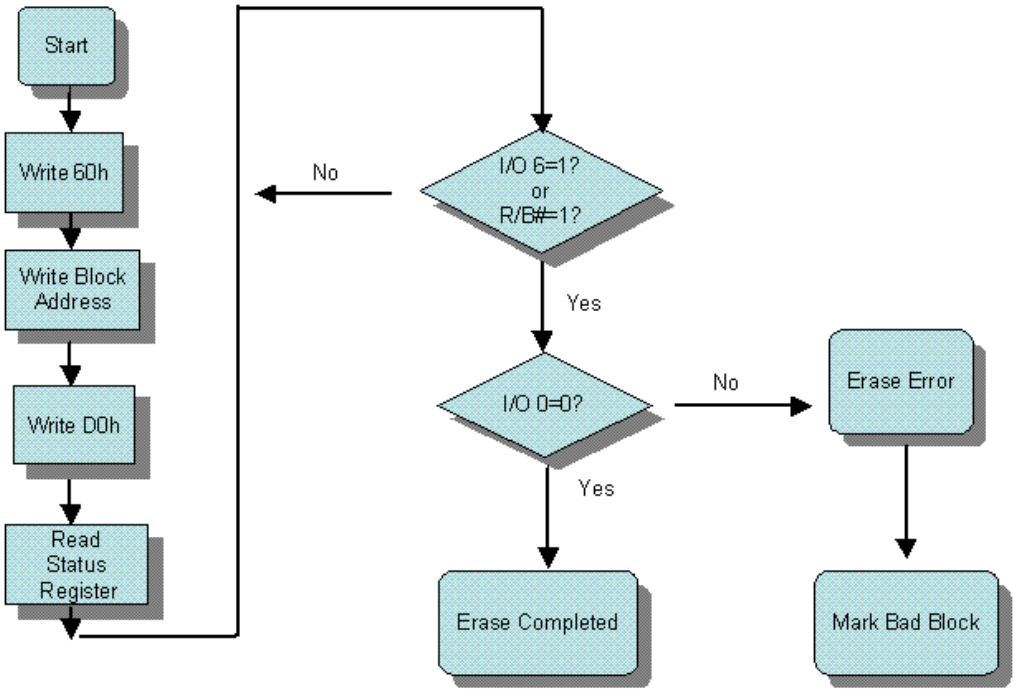
Failure Mode		Detection and Countermeasure sequence
Write	Erase failure	Read Status after Erase → Block Replacement
	Program failure	Read Status after Program → Block Replacement
Read	Up to 4 bits failure	Verify ECC → ECC Correction

NOTE: Error Correcting Code --> RS Code or BCH Code etc.
Example: 4bit / 512 Byte

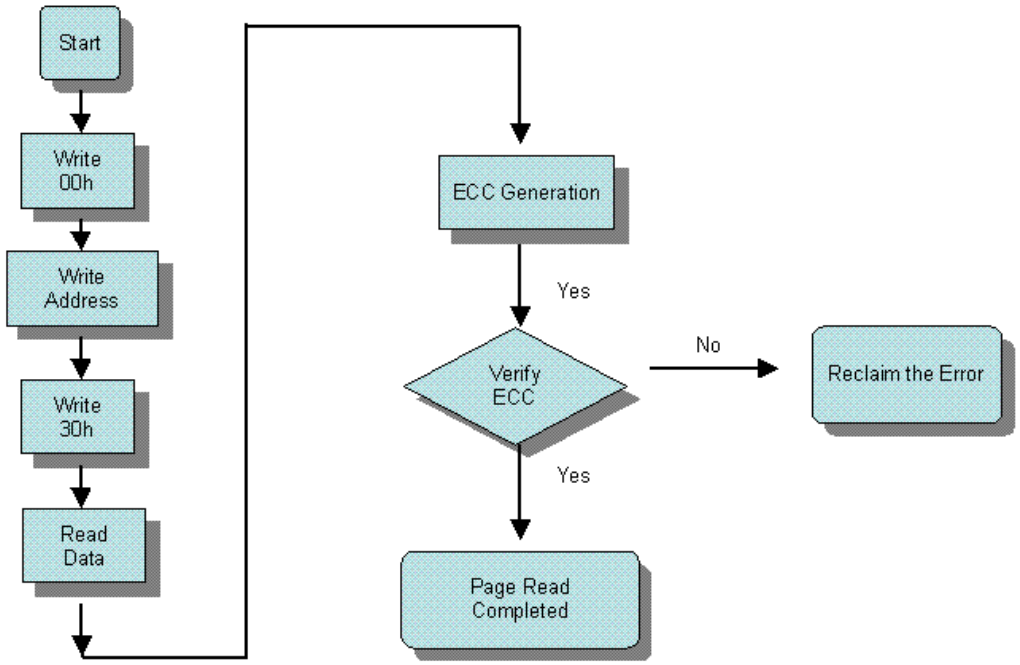
Program Flow Chart



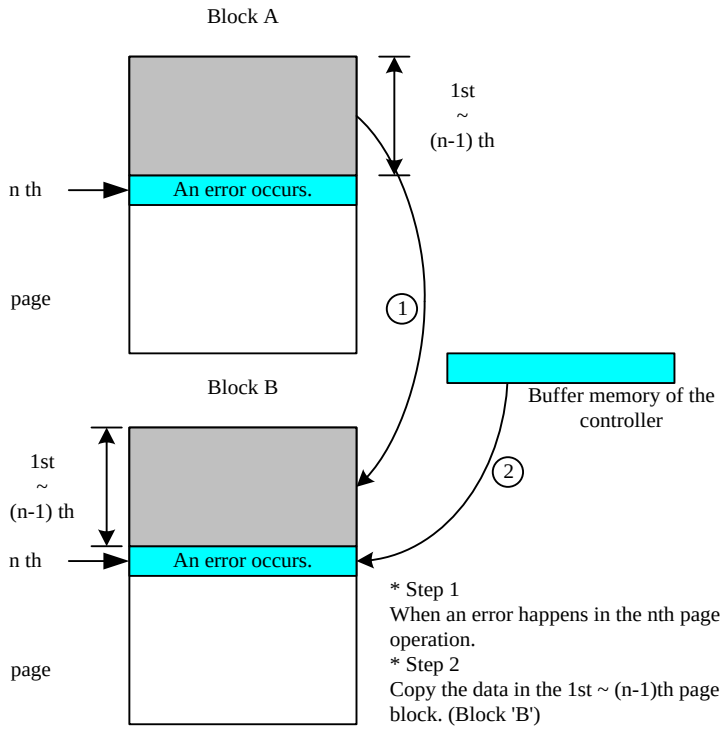
Erase Flow Chart



Read Flow Chart



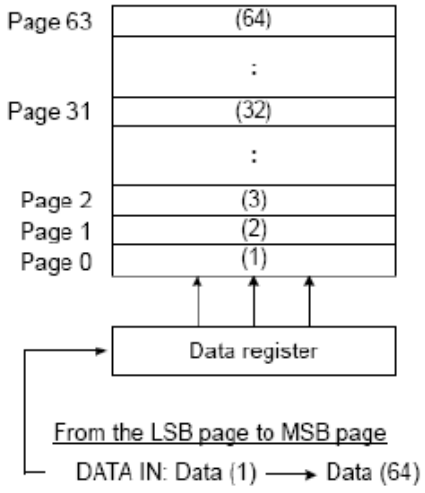
Block Replacement

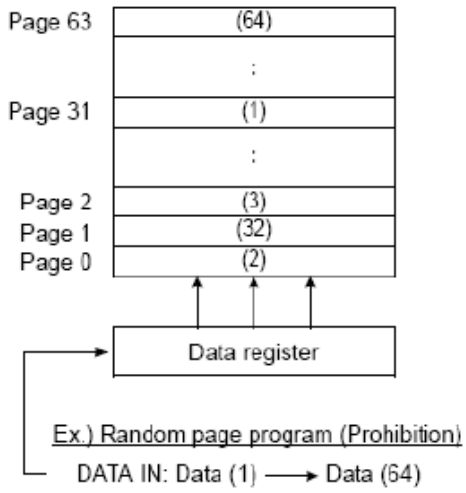


* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





System Interface Using CE# Don't Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112byte (1,056word) data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of μ-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

Program / Read Operation with "CE# **not-care"**

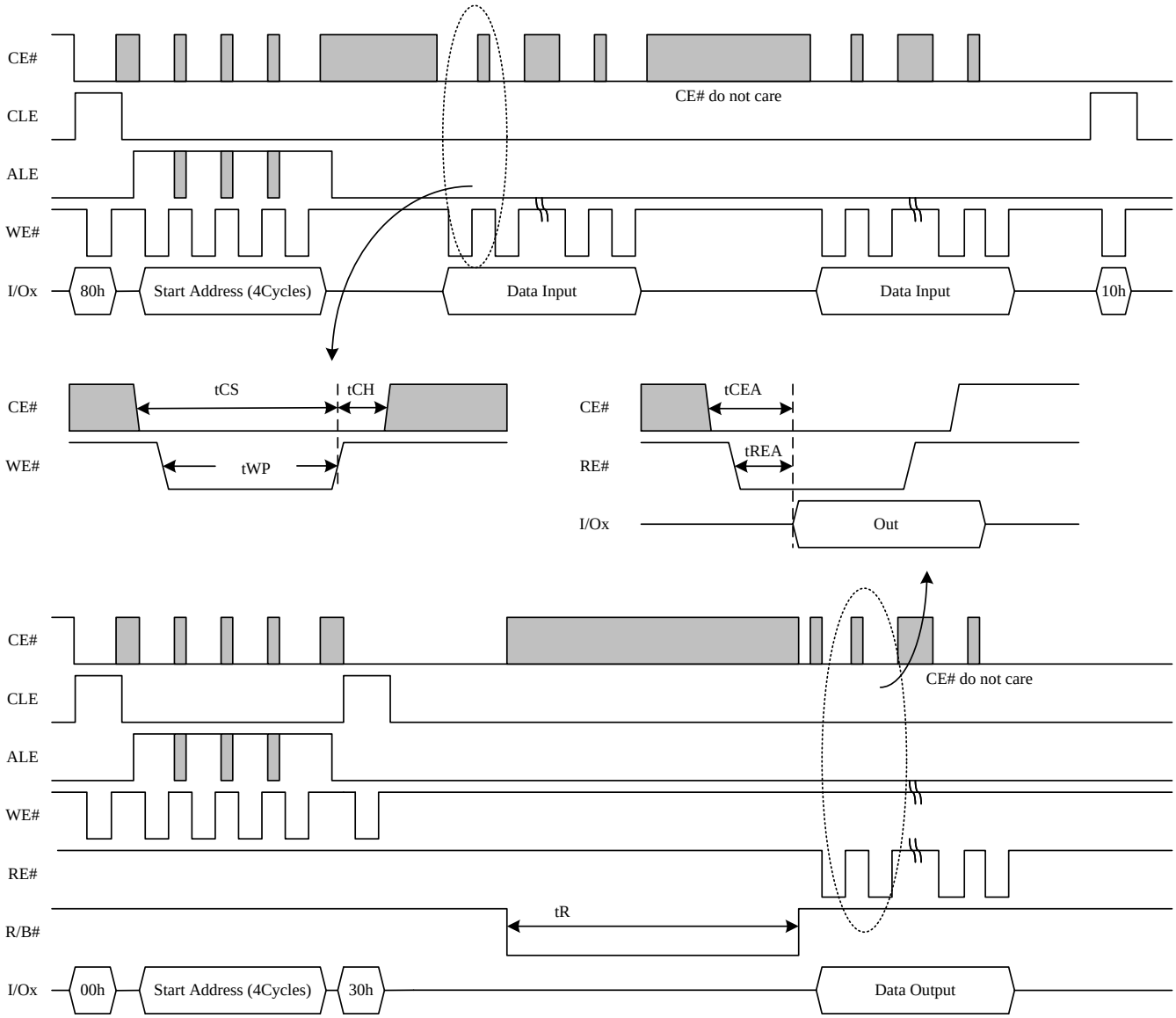


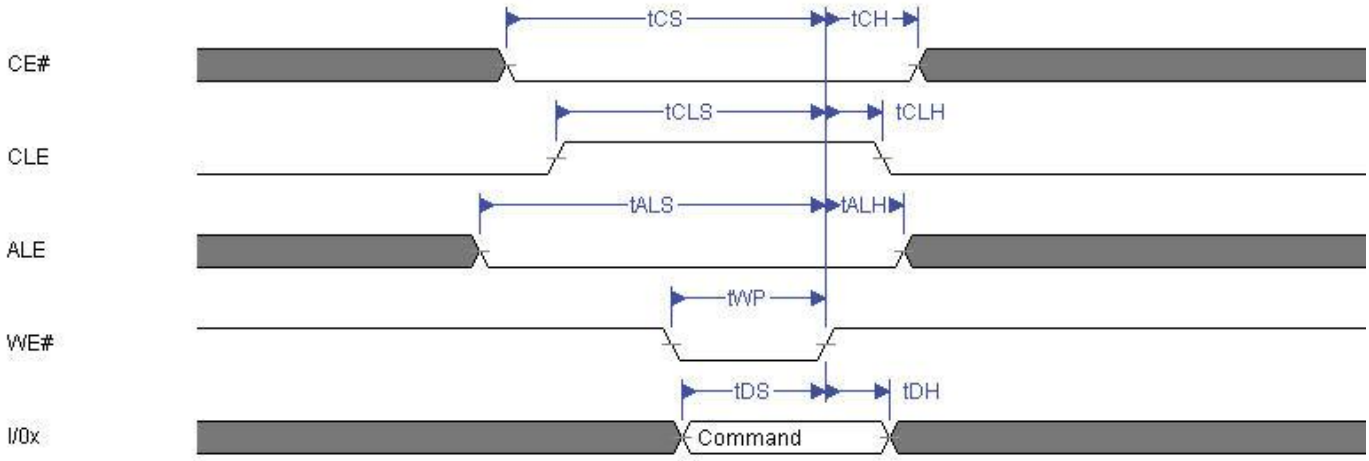
Figure Program/Read Operation with "CE# not-care"

Address Information

Device	Data	I/O	Address			
	Data In/Out	I/Ox	Col. Add1	Col. Add2	Row Add1	Row Add2
F59D1G81MB(x8)	2,112 Byte	I/O 0 ~ I/O 7	A0 ~ A7	A8 ~ A11	A12 ~ A19	A20 ~ A27
F59D1G161MB(x16)	1,056 Word	I/O 0 ~ I/O 15	A0 ~ A7	A8 ~ A10	A11 ~ A18	A19 ~ A26

Timing Diagrams

Command Latch Cycle



Address Latch Cycle

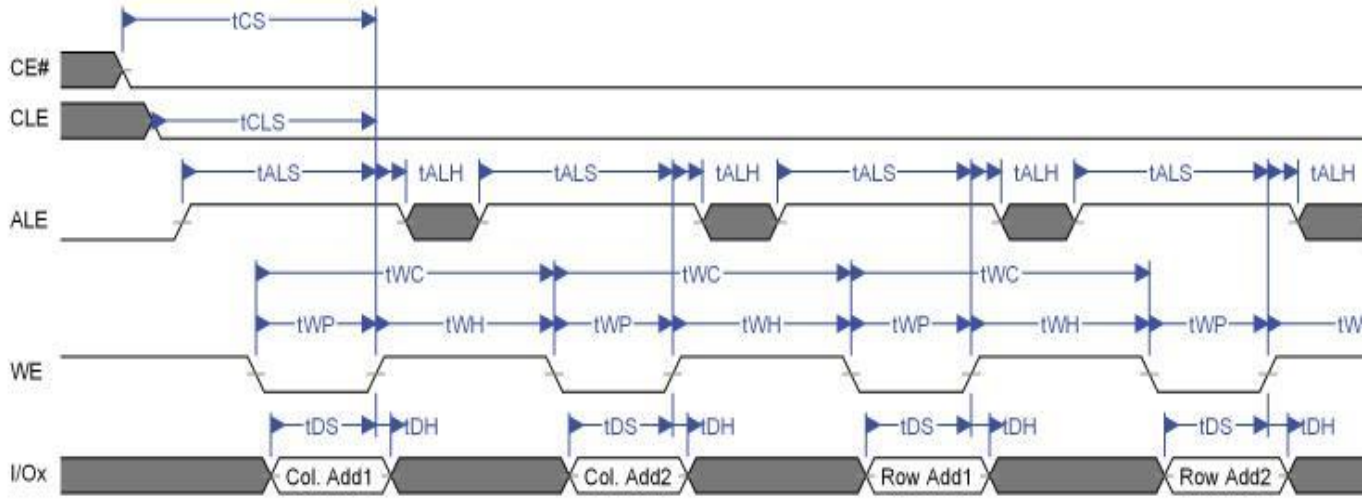


Figure Address Latch Cycle

Input Data Latch Cycle

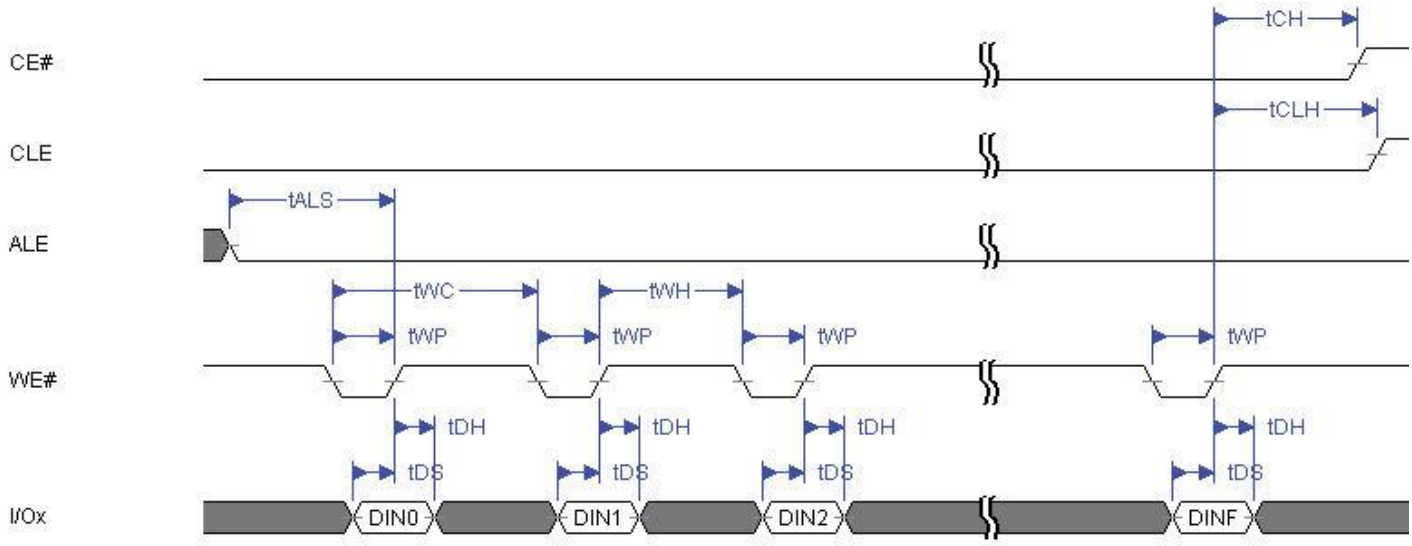


Figure Input Data Latch Cycle

Serial Access Cycle after Read (CLE = L, WE#= H, ALE = L)

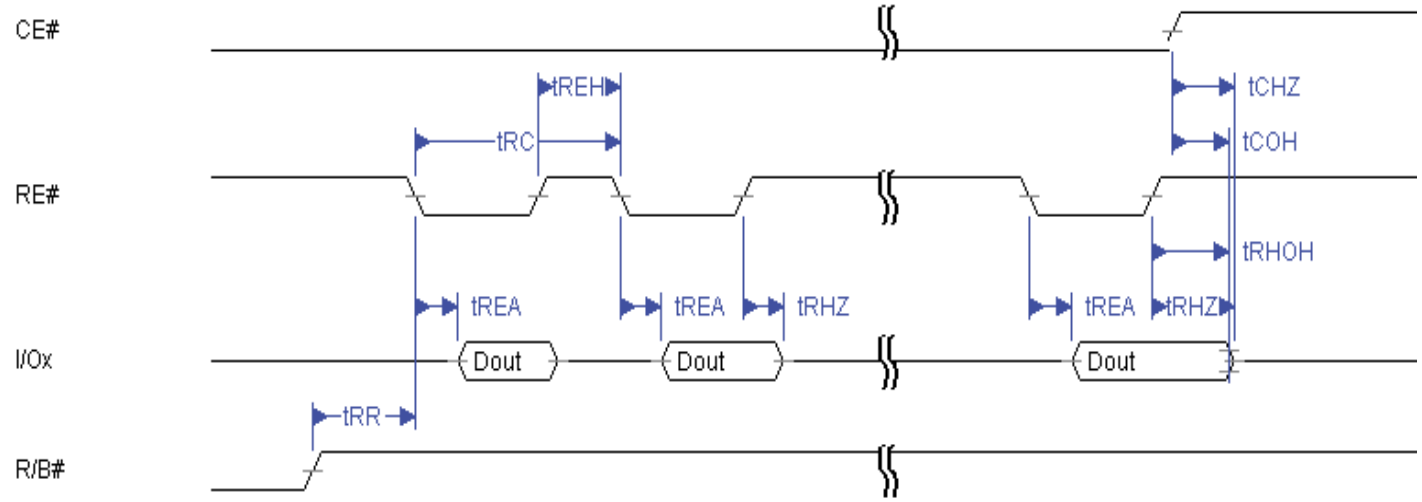


Figure Sequential Out Cycle after Read

NOTE:
1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

Serial Access Cycle after Read (EDO Type CLE = L, WE# = H, ALE = L)

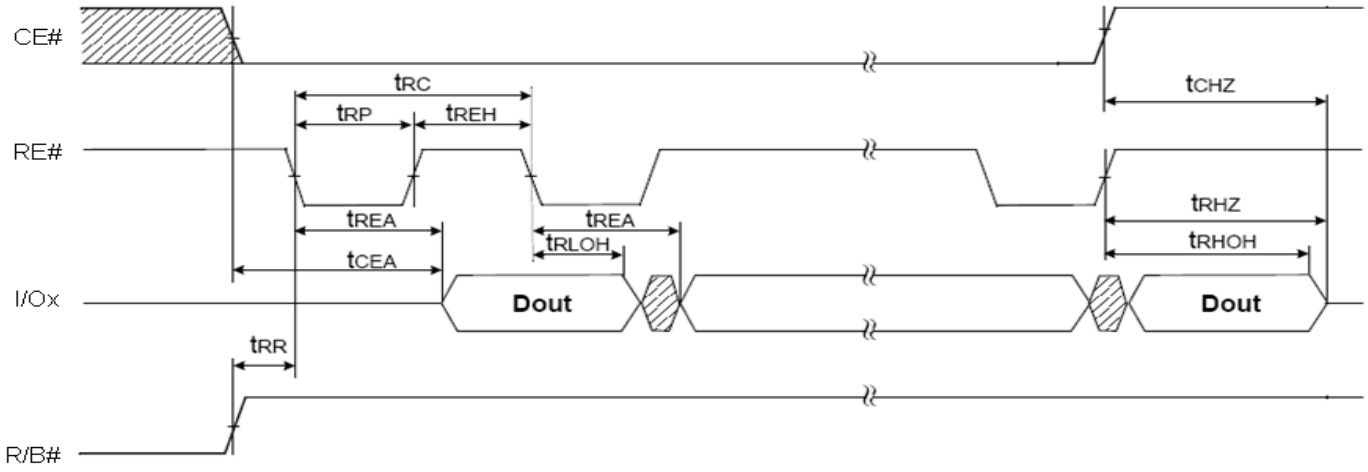


Figure Sequential Out Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)

NOTE:
1. Transition is measured at +/-200mV from steady state voltage with load.
   This parameter is sample and not 100% tested. (t_{CHZ}, t_{RHZ})
2. t_{RLOH} is valid when frequency is higher than 20MHZ.
   t_{RHOH} starts to be valid when frequency is lower than 20MHZ.

Status Read Cycle

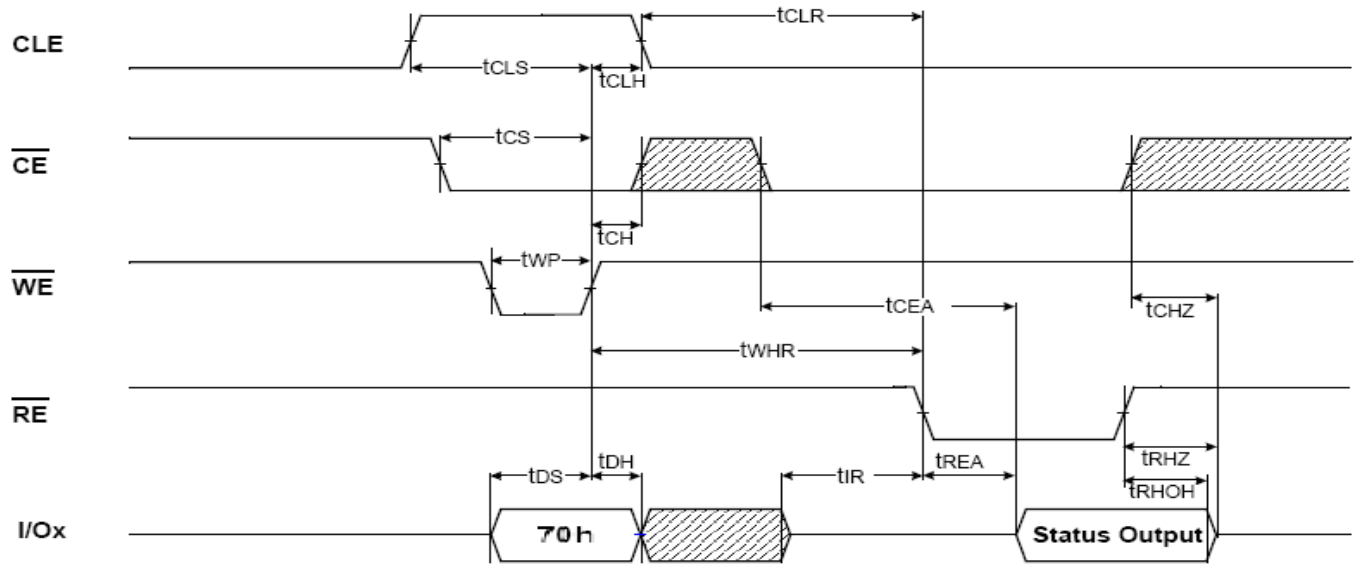


Figure Status Read Cycle

Read Operation

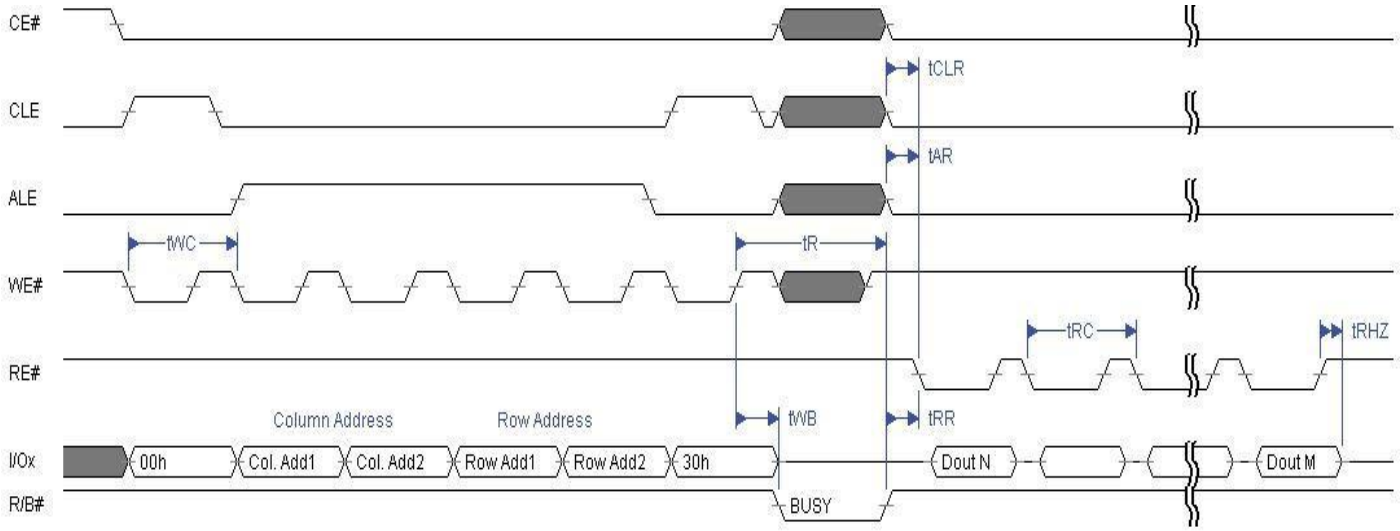


Figure Read Operation (Read One Page)

Read Operation (Intercepted by CE#)

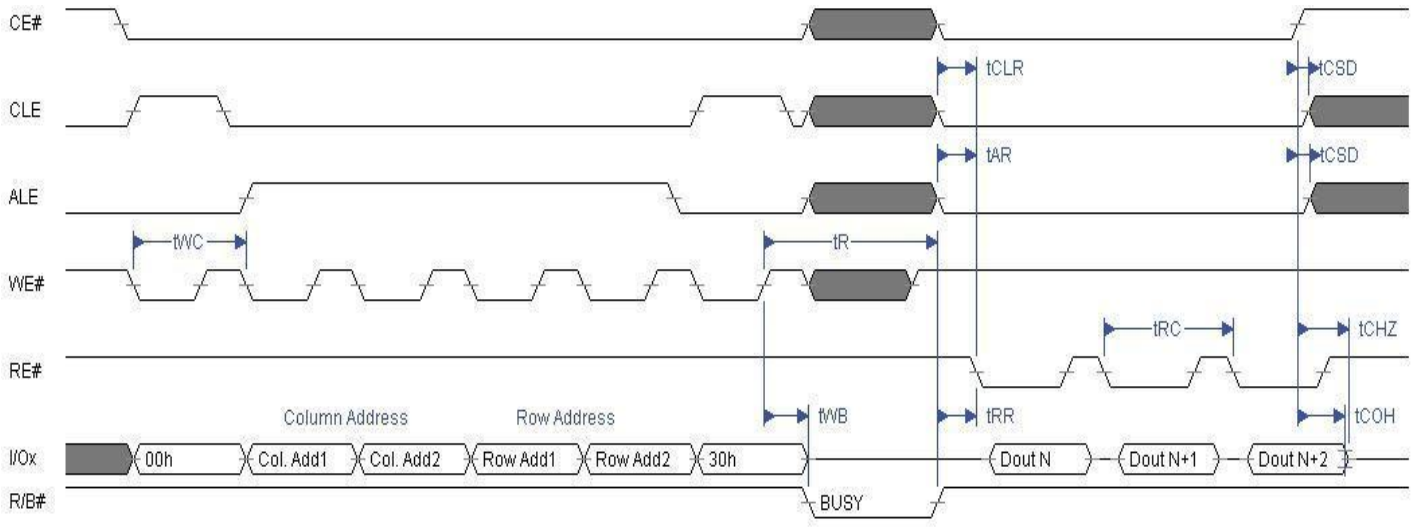


Figure Read Operation Intercepted by CE#

Random Data Output In a Page

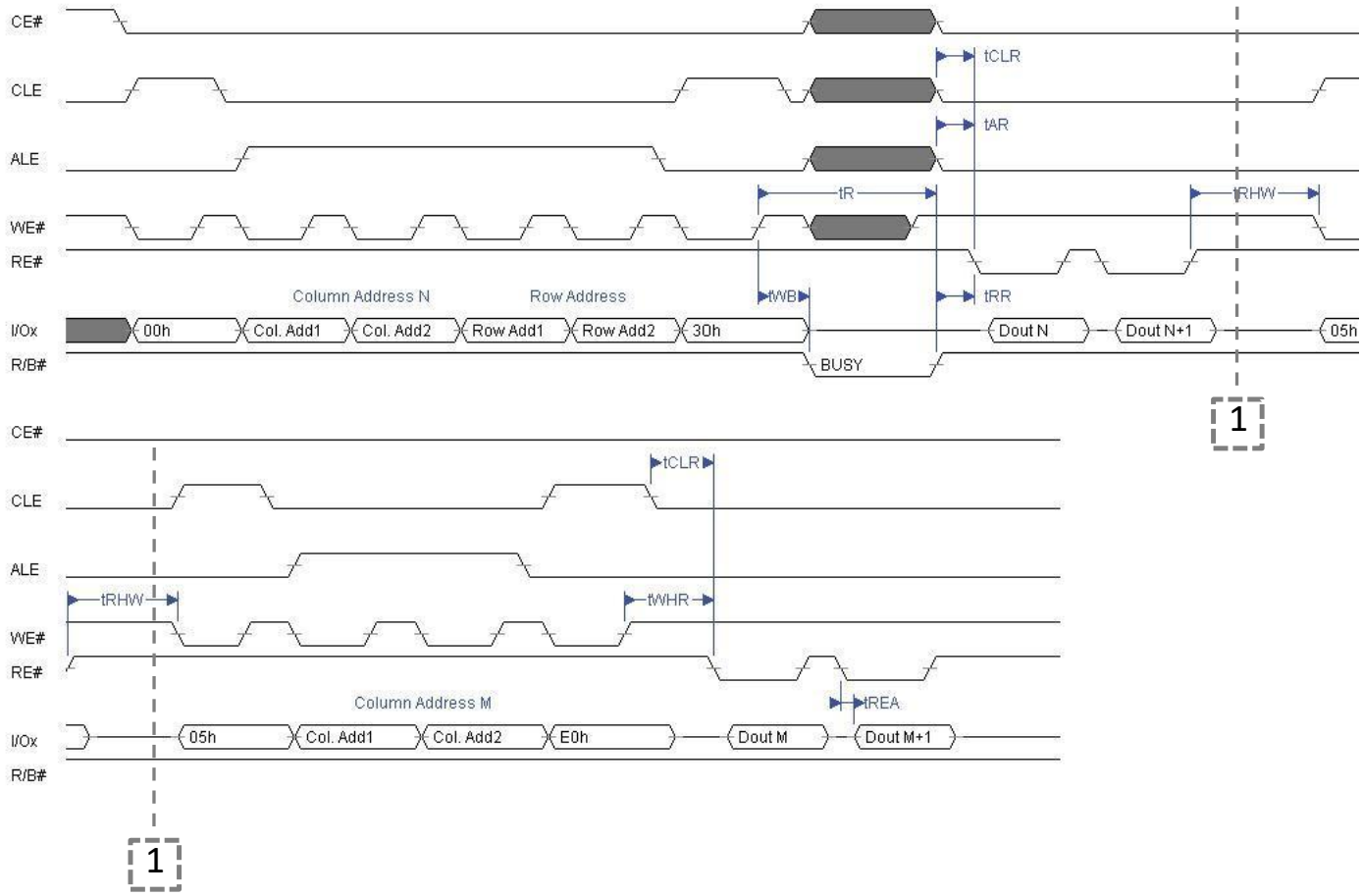


Figure Random Data Output

Page Program Operation

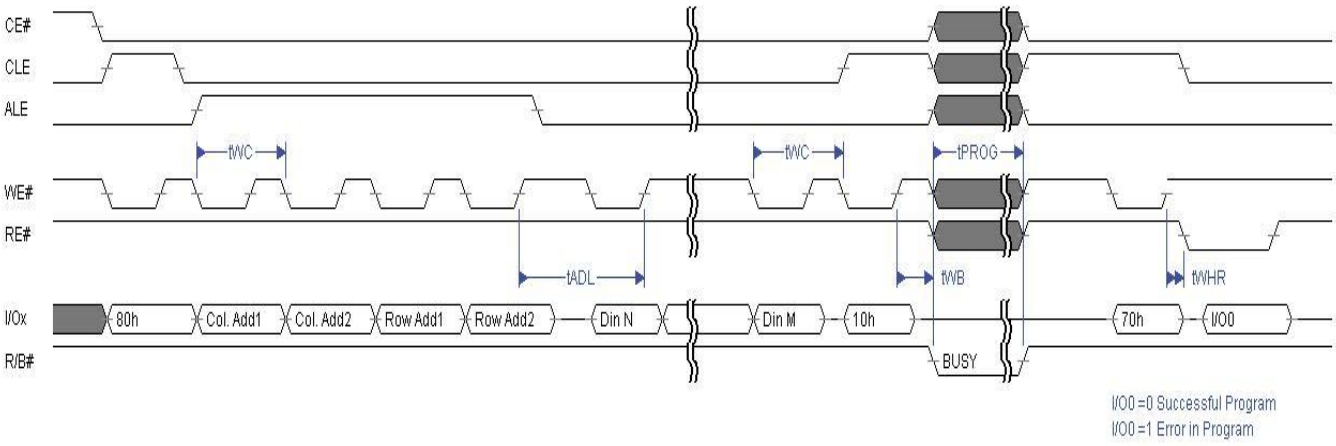


Figure Page Program Operation

Page Program Operation with Random Data Input

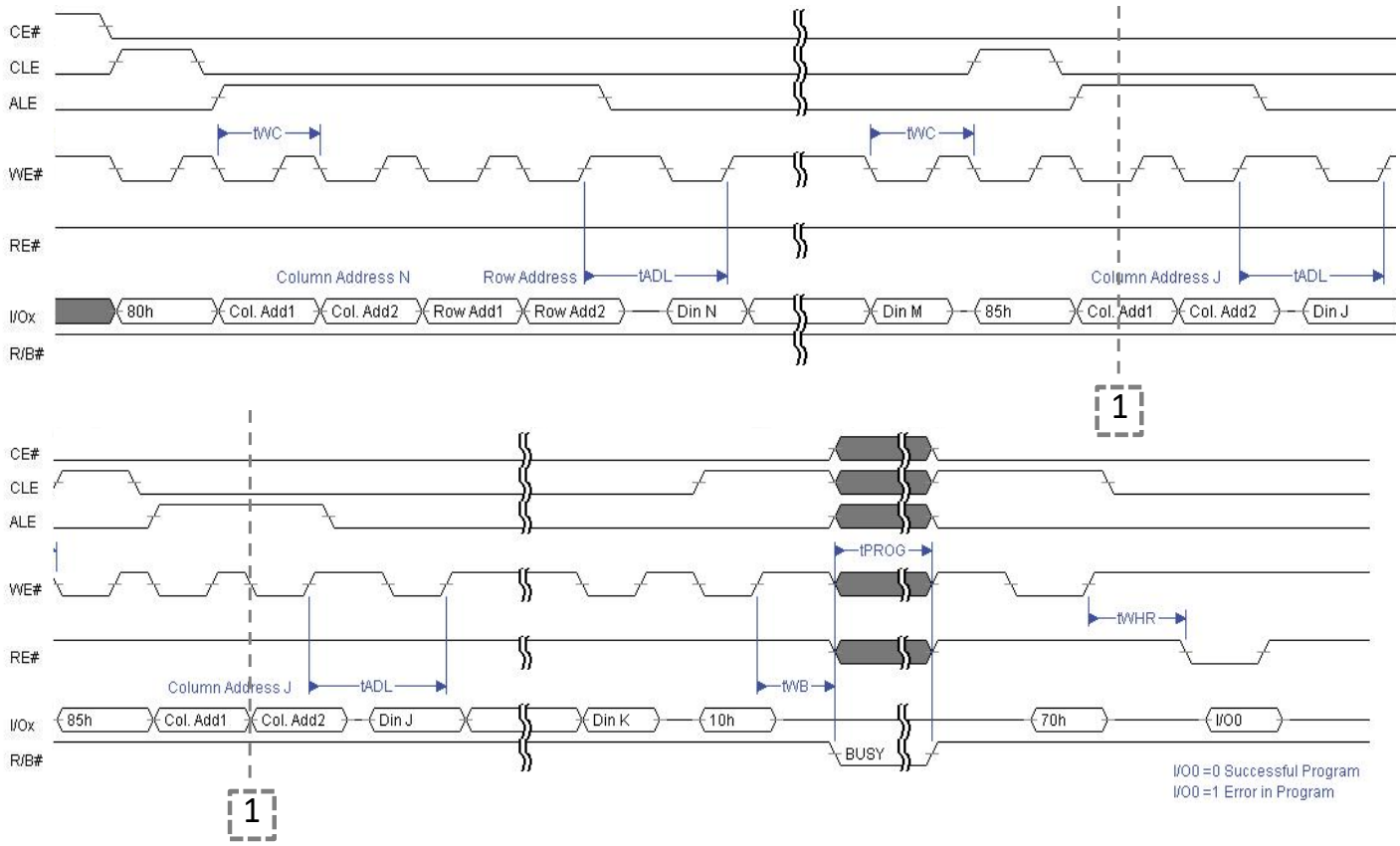


Figure Random Data Input

NOTE: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

Copy-Back Operation with Random Data Input

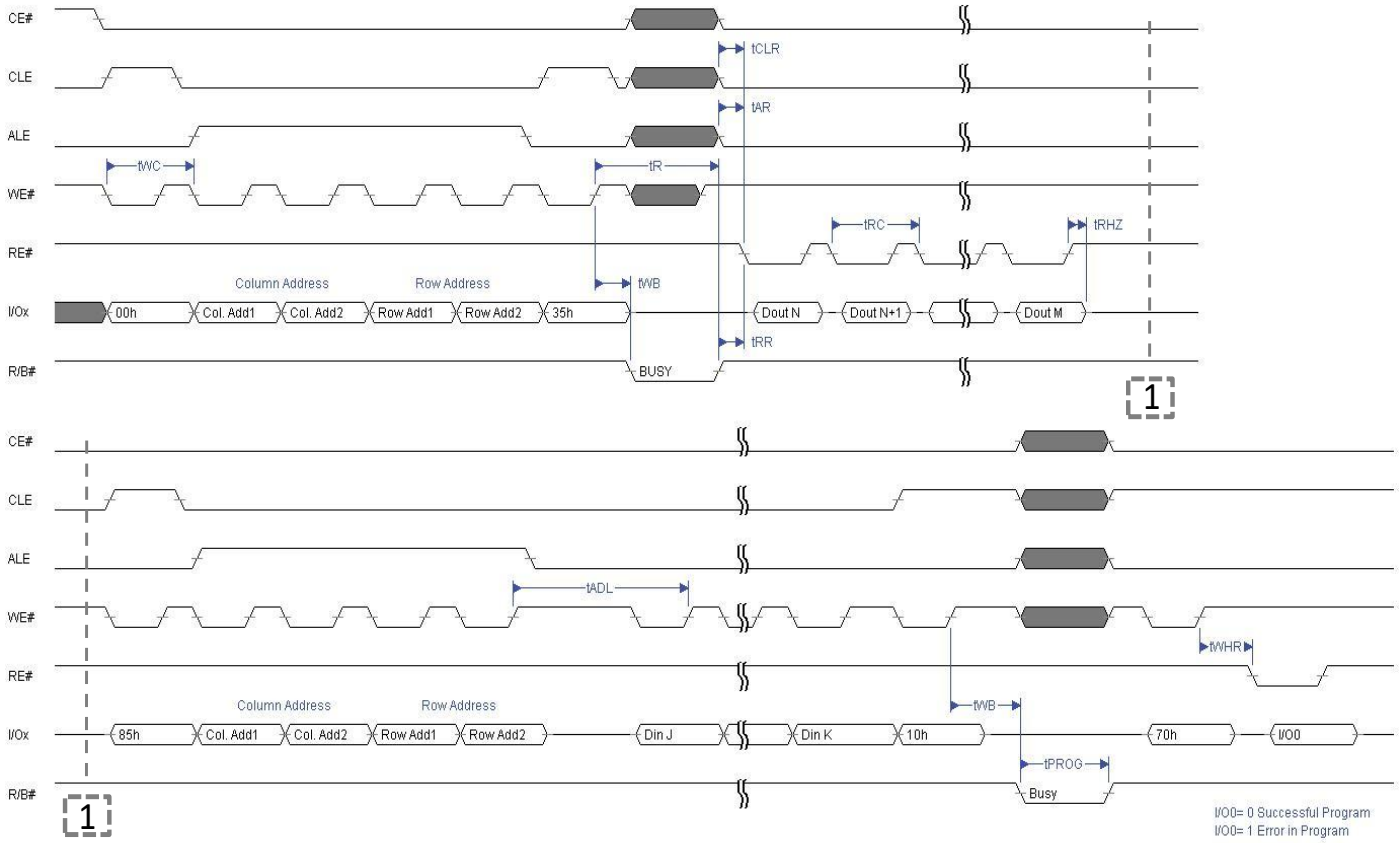


Figure Copy-Back Operation with Random Data Input

Cache Program Operation

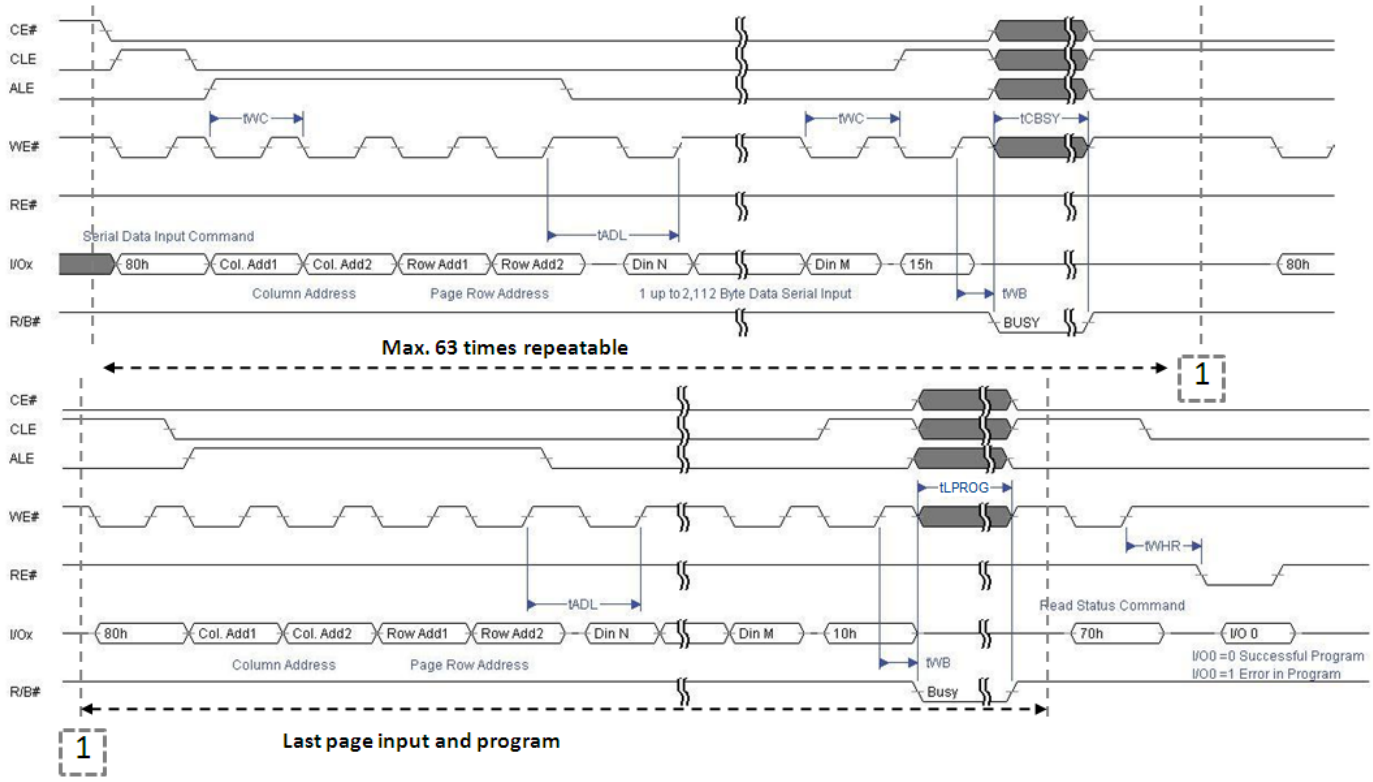


Figure Cache Program Operation

Cache Read Operation

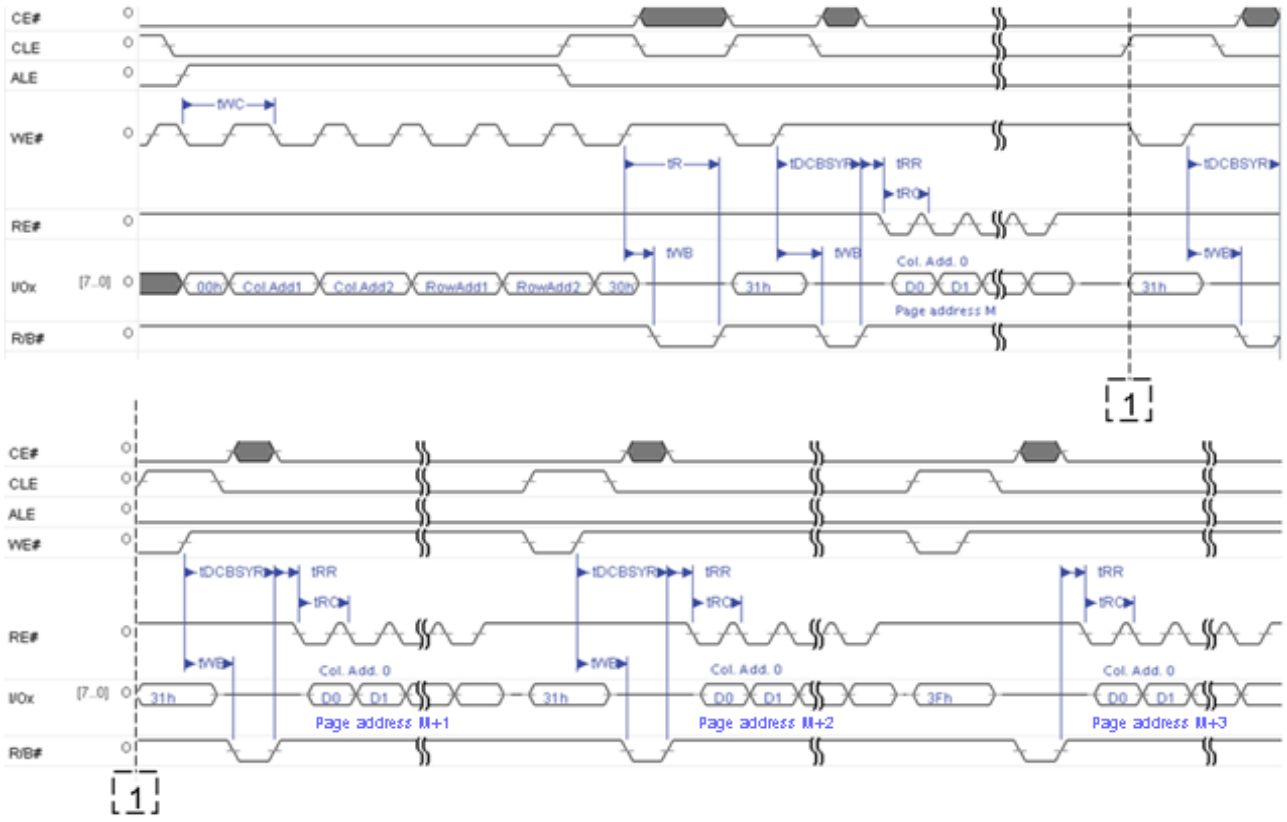


Figure Cache Read Operation

Block Erase Operation

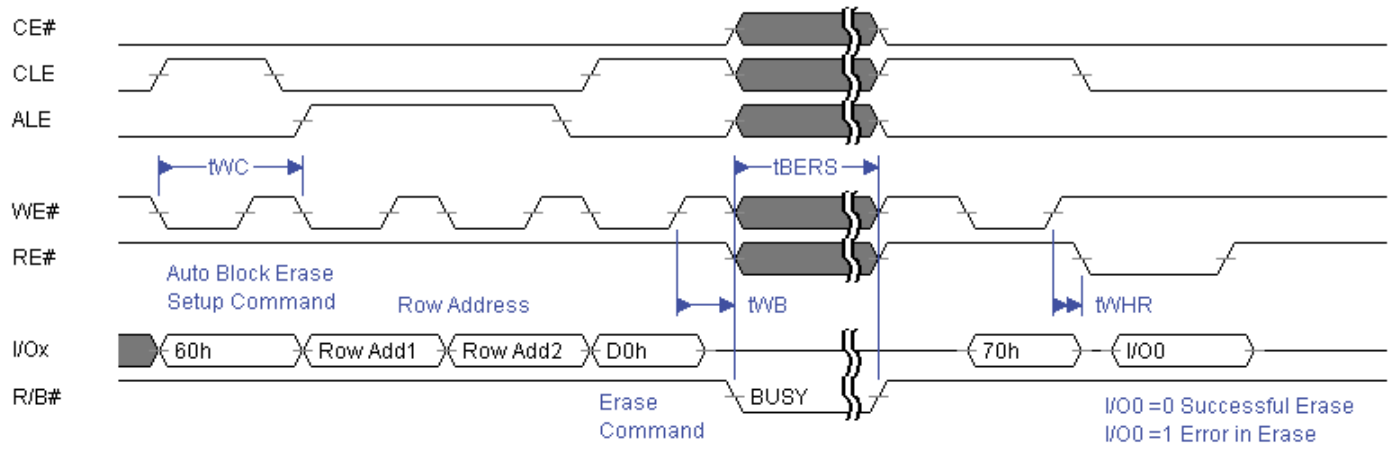


Figure Block Erase Operation

Read ID Operation

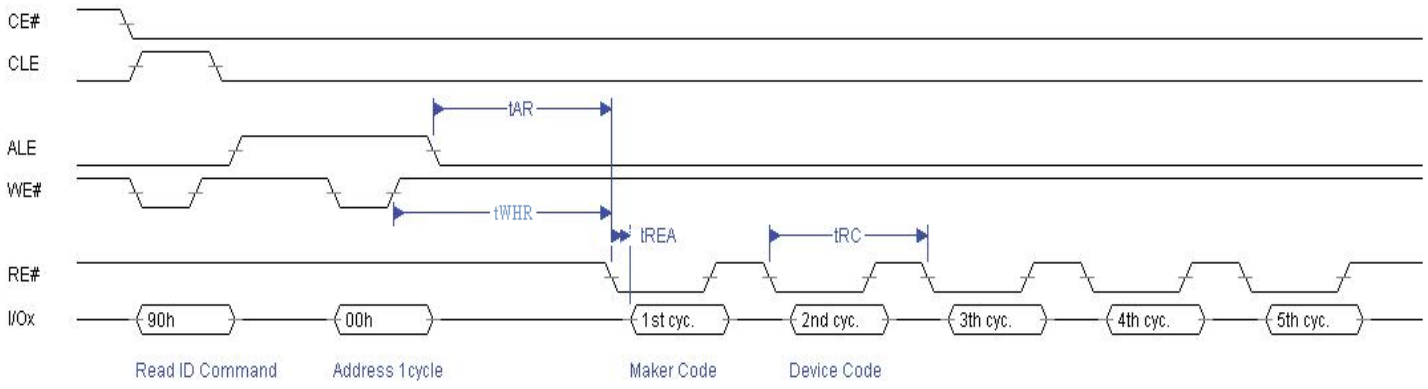


Figure Read ID Operation (00h Address)

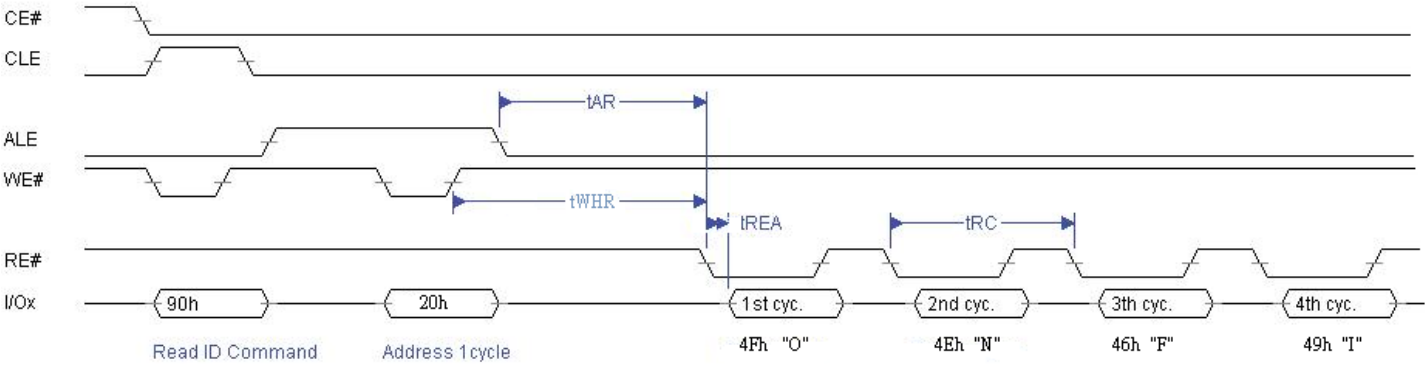


Figure Read ID Operation (20h Address)

ID Definition Table

00h Address

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle	6th ~ 9th Cycle
F59D1G81MB (X8)	C8h	**61h**	80h	15h	40h	7Fh
F59D1G161MB (X16)	C8h	**71h**	80h	55h	40h	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, etc
4th Byte	Page Size, Block Size, etc
5th Byte	Plane Number, Plane Size
6th Byte	JEDEC Maker Code Continuation Code, 7Fh
7th Byte	JEDEC Maker Code Continuation Code, 7Fh
8th Byte	JEDEC Maker Code Continuation Code, 7Fh
9th Byte	JEDEC Maker Code Continuation Code, 7Fh

3rd ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between Multiple Chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

4th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Redundant Area Size (Byte/512Byte)	8						0		
	16						1		
Block Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Organization	X8		0						
	X16		1						
Serial Access Time	45ns	0				0			
	Reserved	0				1			
	25ns	1				0			
	Reserved	1				1			

5th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	4bit/512B							0	0
	2bit/512B							0	1
	1bit/512B							1	0
	Reserved							1	1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size(without Redundant Area)	64Kb		0	0	0				
	128Kb		0	0	1				
	256Kb		0	1	0				
	512Kb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved	Reserved	0							

6th ~ 9th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
JEDEC Maker Code Continuation Code	7F	0	1	1	1	1	1	1	1

Device Operation

Page Read

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, four-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 2,112Byte of data on a page are transferred to cache registers via data registers within 25us (tR). Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 25ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

A page read sequence is illustrated in Figure below, where column address, page address are placed in between commands 00h and 30h. After tR read time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 30h. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.

Read Operation

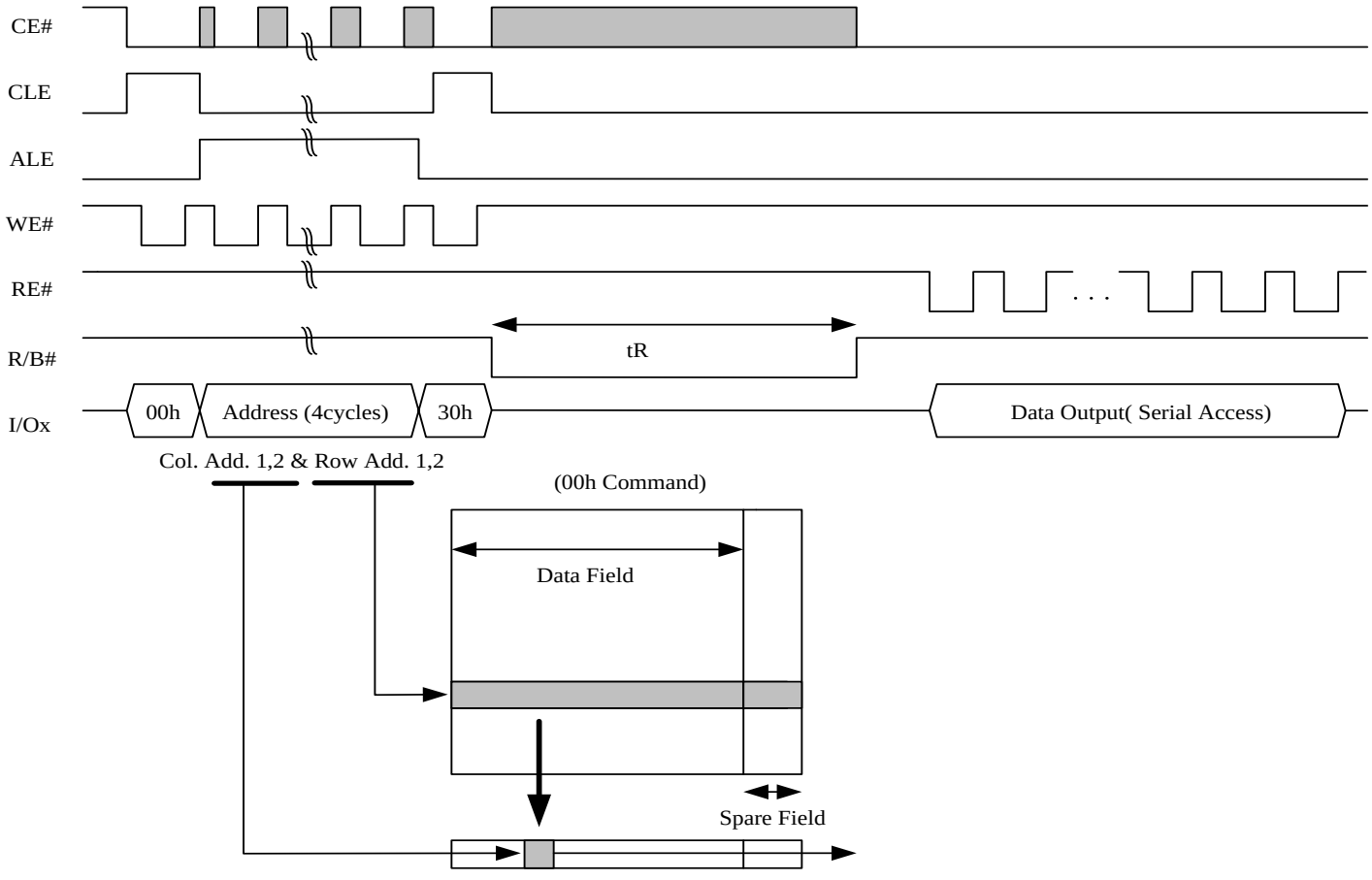
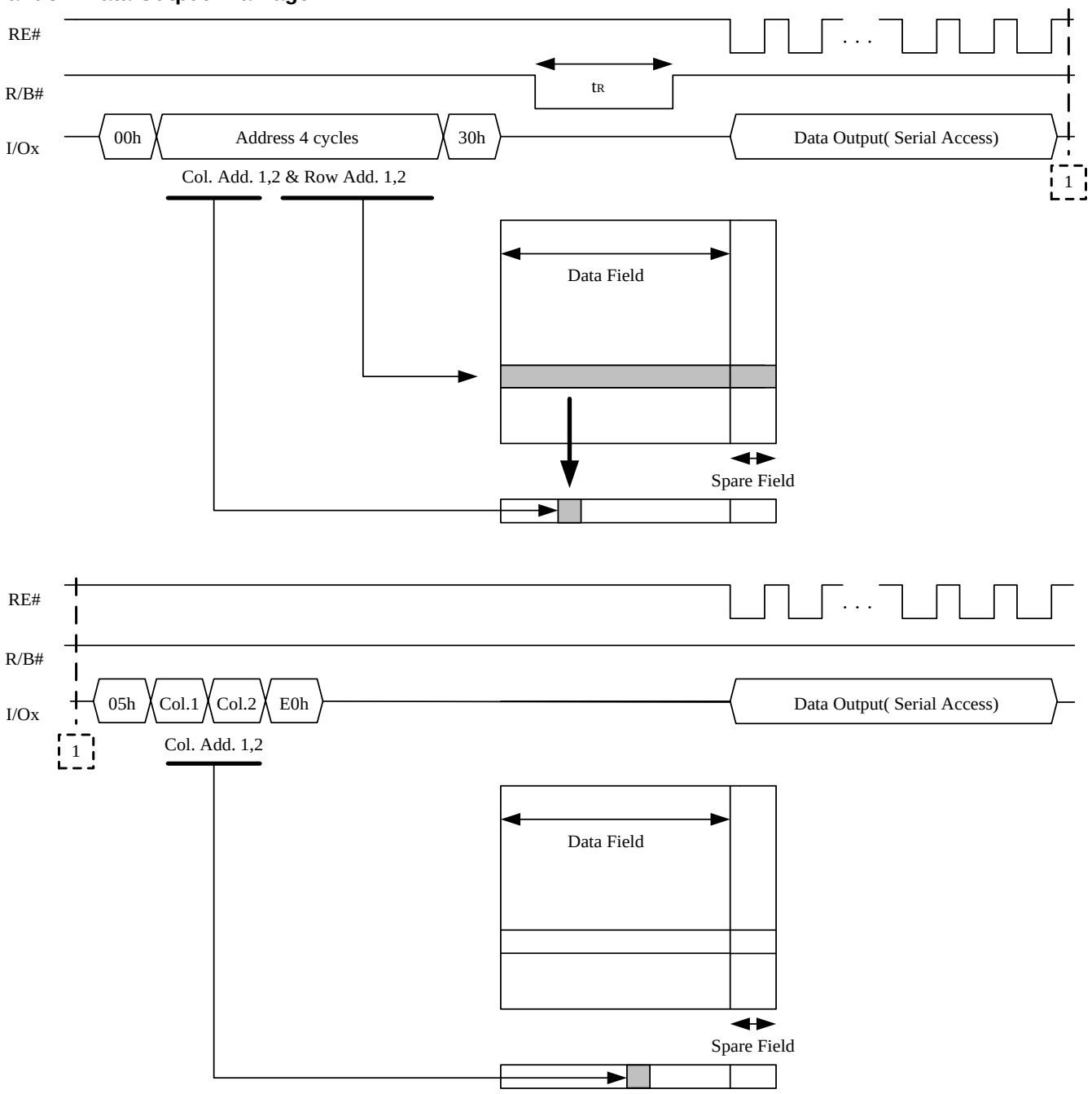


Figure Read Operation

Random Data Output In a Page



Page Program

The device is programmed based on the unit of a page. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 2,112byte of data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

The serial data input cycle begins with the Serial Data Input command (80h), followed by a four-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in Figure below, where column address, page address, and data input are placed in between 80h and 10h. After tPROG program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.

Program & Read Status Operation

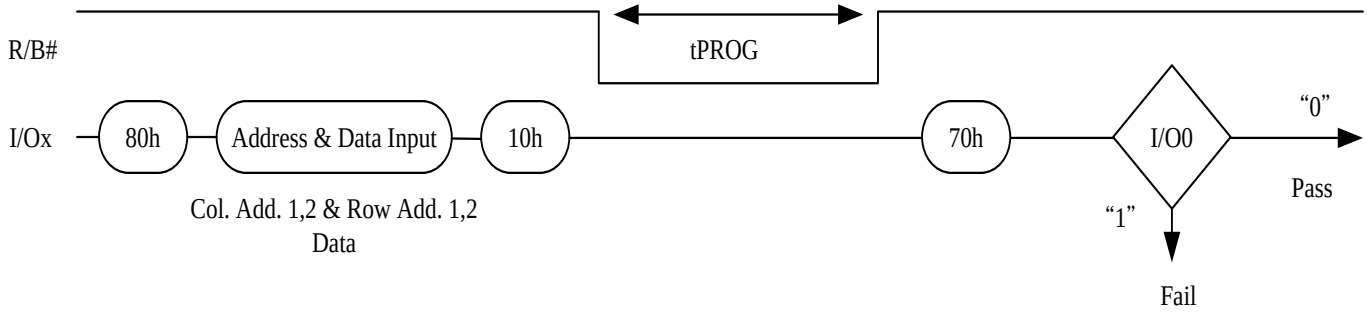


Figure Program & Read Status Operation

Random Data Input In a Page

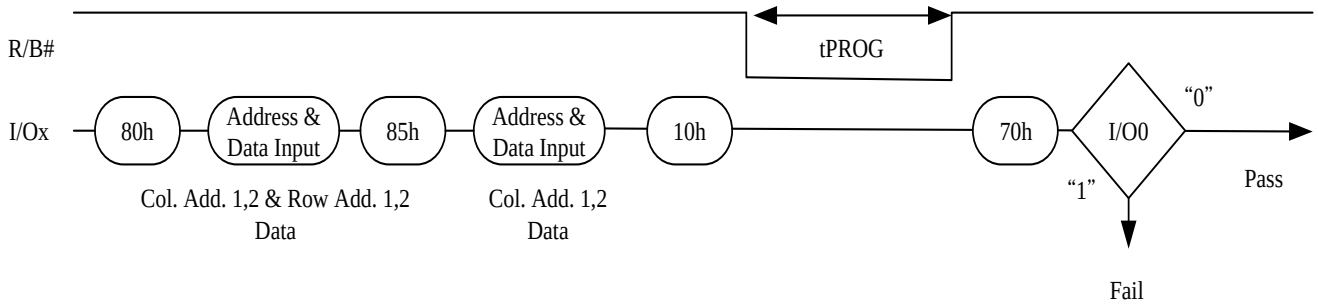


Figure Random Data Input In a Page

Cache Program

Cache Program is an extension of Page Program, which is executed with 2,112 byte(x8) data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2,112 bytes(x8) into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identity the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

Cache Program (available only within a block)

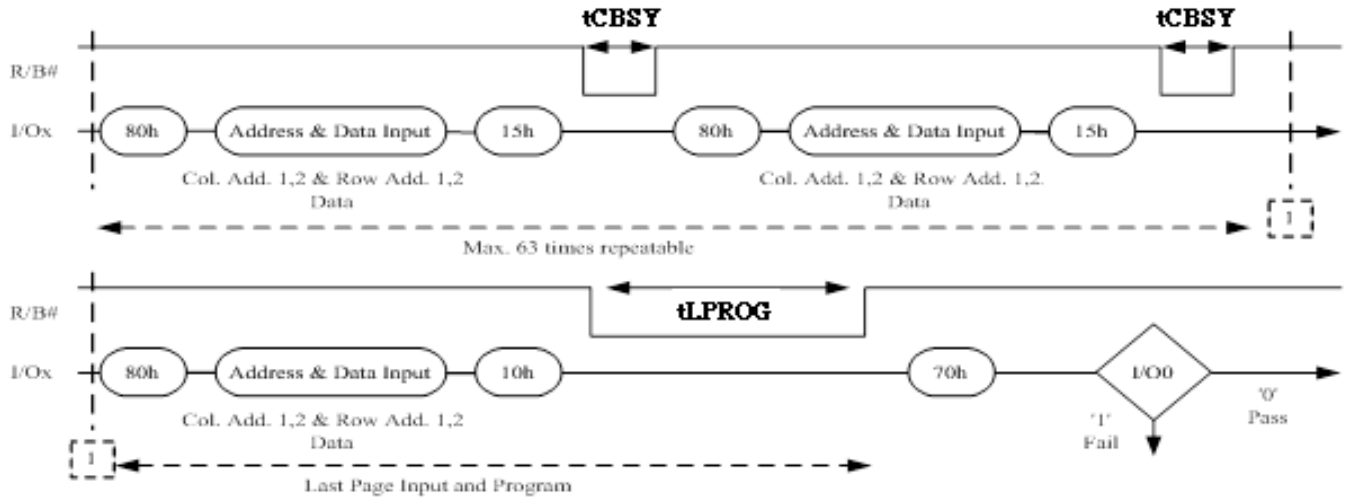


Figure Cache Program

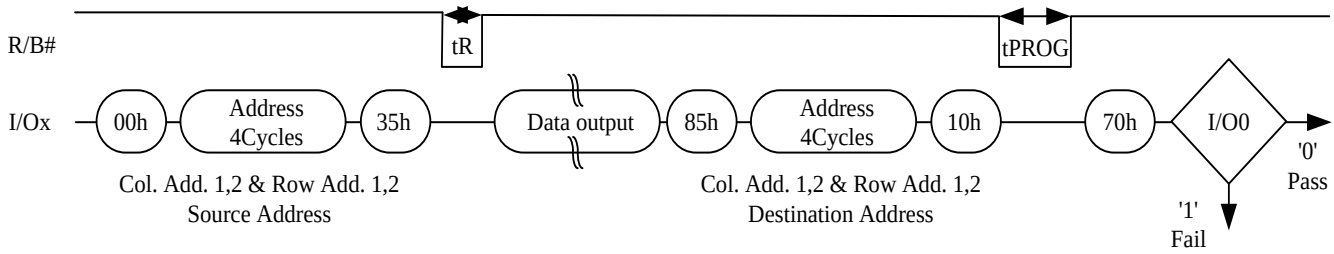
NOTE:

1. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.
2. t_{LPROG} = Program time for the last page + Program time for the (last-1)th page – (Program command cycle time + Last page data loading time)

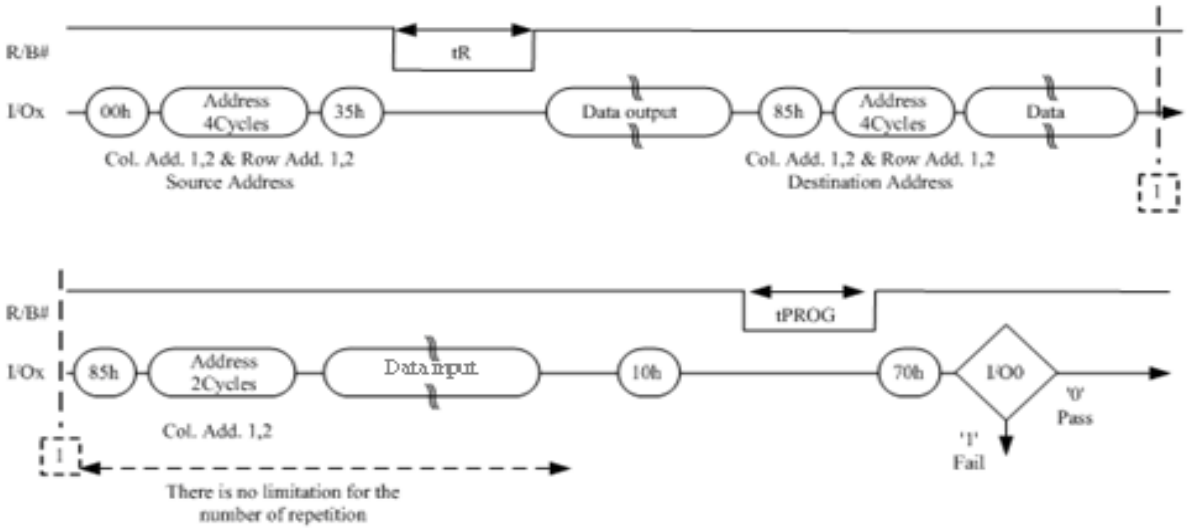
Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with “35h” command and the Source address moves the whole 2,112byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in Figure below. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.

Page Copy-Back Program Operation



Page Copy-Back Program Operation with Random Data Input

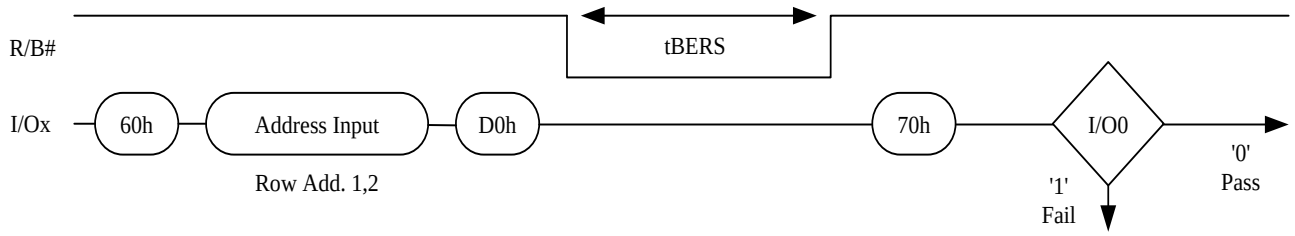


Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a two-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise.

At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. Figure below illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After tBERS erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.

Block Erase Operation



Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

Status Register Definition for 70h Command

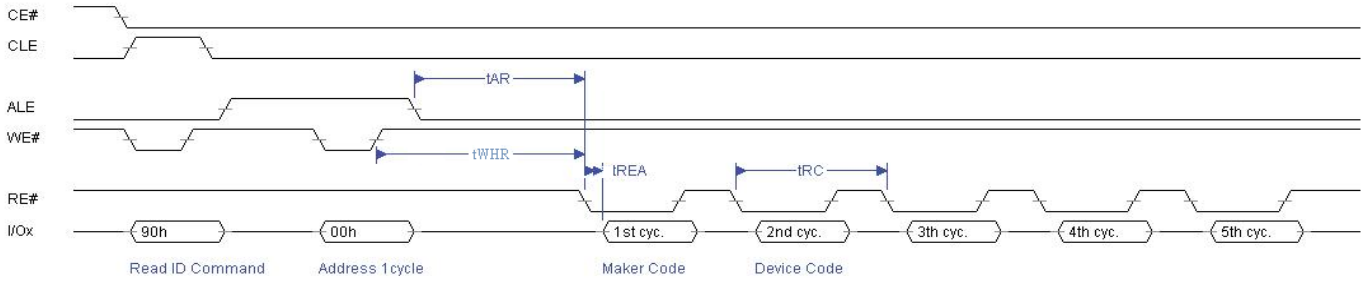
I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O0	Pass / Fail	Pass / Fail	Pass / Fail (N)	NA	NA	Pass: 0 Fail: 1
I/O1	NA	NA	Pass / Fail (N-1)	NA	NA	Pass: 0 Fail: 1
I/O2	NA (Pass/Fail, OTP)	NA	NA	NA	NA	Don't cared
I/O3	NA	NA	NA	NA	NA	Don't cared
I/O4	NA	NA	NA	NA	NA	Don't cared
I/O5	NA	NA	True Ready / Busy	NA	True Ready / Busy	Busy: 0 Ready: 1
I/O6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Busy: 0 Ready: 1
I/O7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: 0 Not Protected: 1

NOTE:
1. I/Os defined 'NA' are recommended to be masked out when Read Status is being executed.
2. n: current page, N-1: previous page

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

Read ID Operation



ID Definition Table

Product ID	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
F59D1G81MB (x8)	C8h	61h	80h	15h	40h
F59D1G161MB (x16)	C8h	71h	80h	55h	40h

Table ID Definition Table (00h)

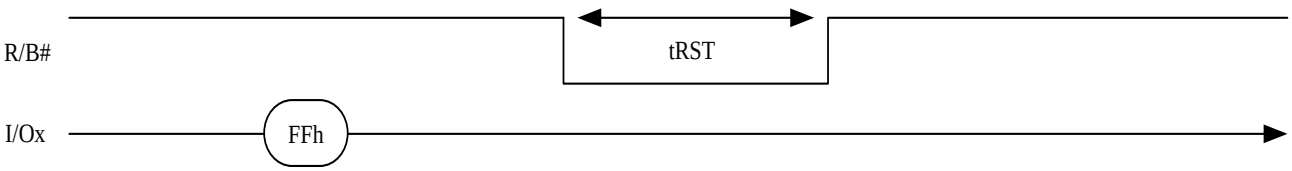
Product ID	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle
F59D1G81MB (x8)	4Fh	4Eh	46h	49h
F59D1G161MB (x16)	4Fh	4Eh	46h	49h

Table ID Definition Table (20h)

Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP#is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for t_{RST} after the Reset command is written. Refer to Figure below.

Reset Operation



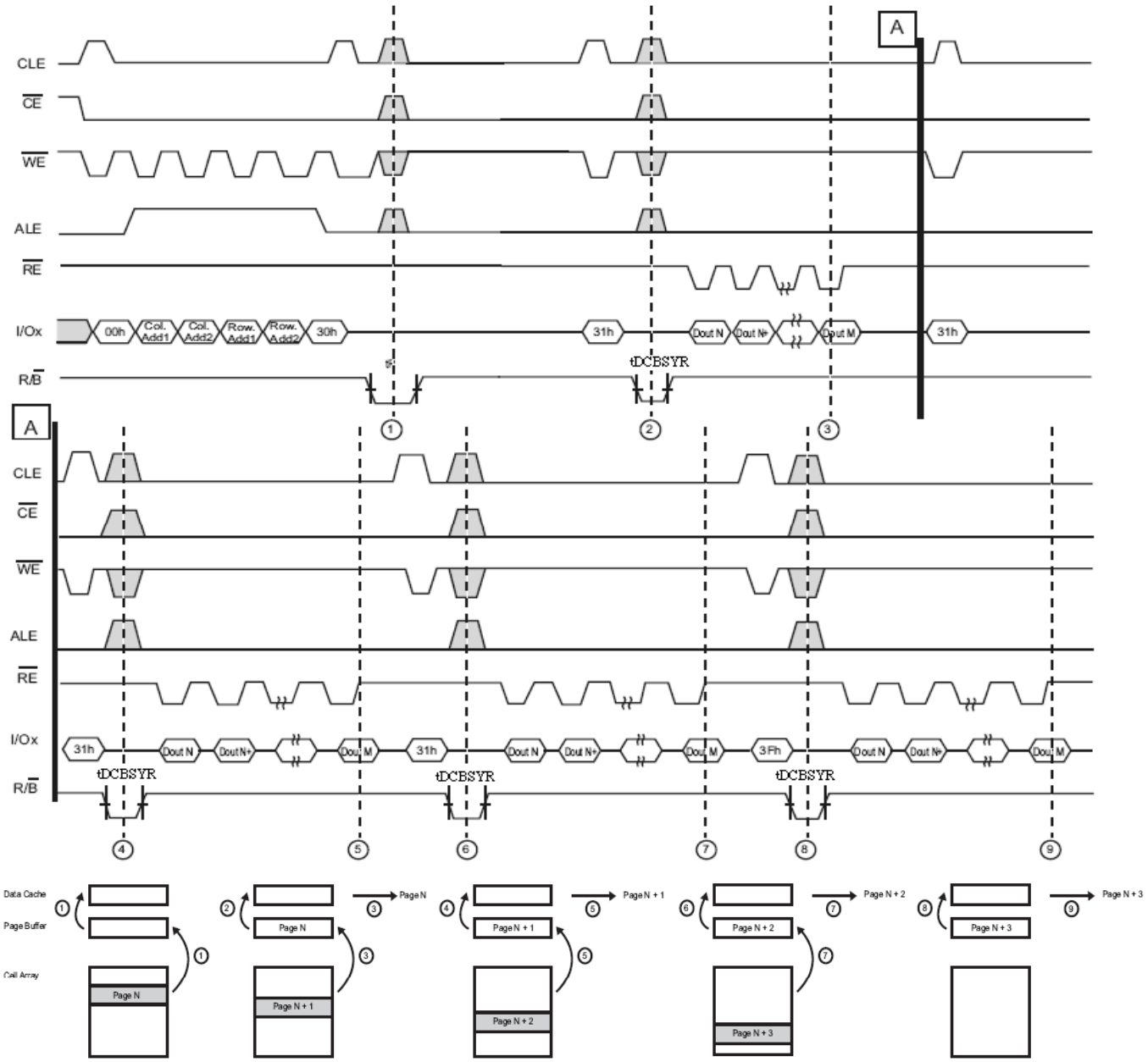
Device Status Table

	After Power-up	After Reset
Operation Mode	00h Command is latched	Waiting for next command

Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of t_{DCBSYR}, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

Read Operation with Cache Read



Ready / Busy#

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transition to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

Ready/Busy# Pin Electrical Specifications

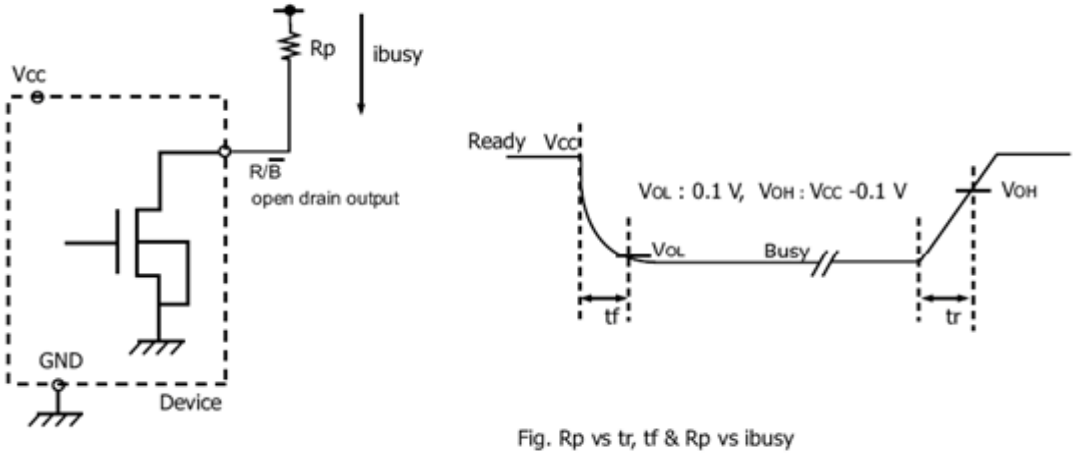
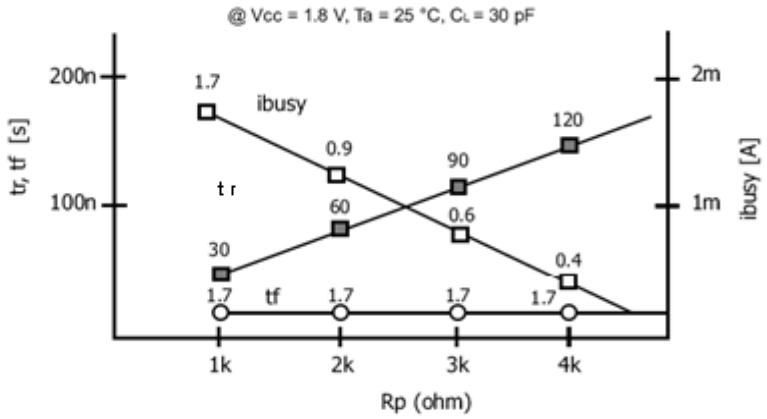


Fig. Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{1.85\ V}{3\ mA + \sum I_L}$$

where IL is the sum of the iput currents of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power Up Sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

AC Waveforms for Power Transition

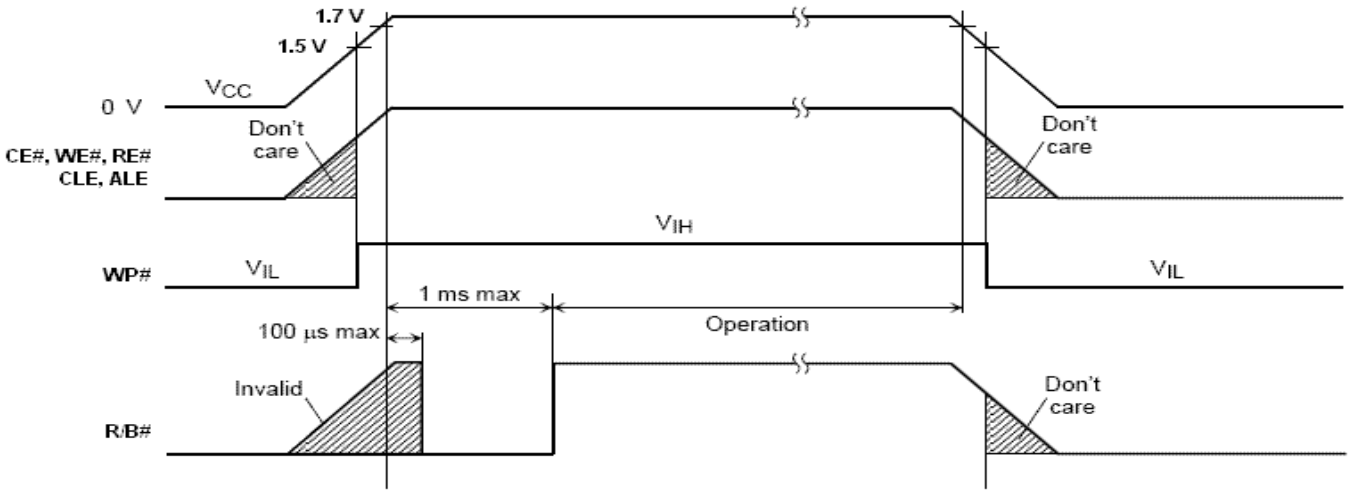
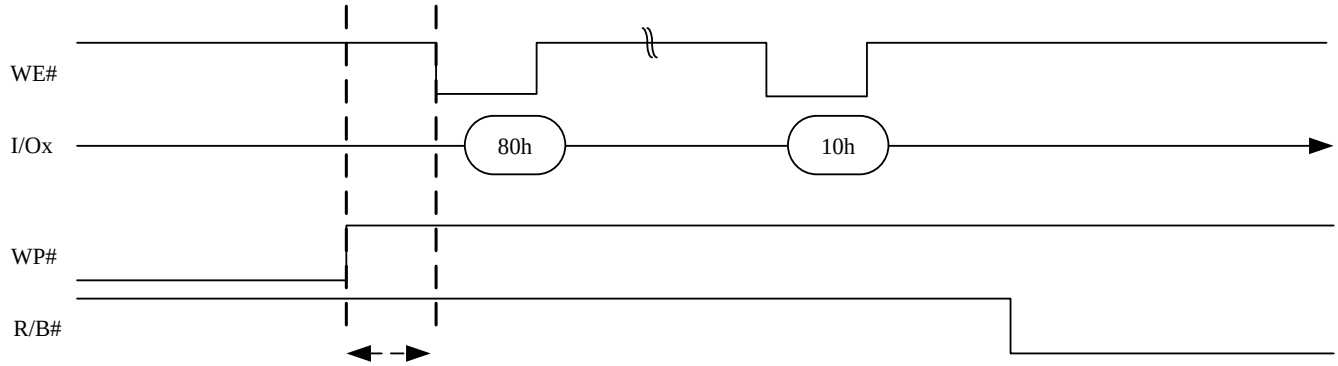


Figure AC Waveforms for Power Transition

Write Protect Operation

Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

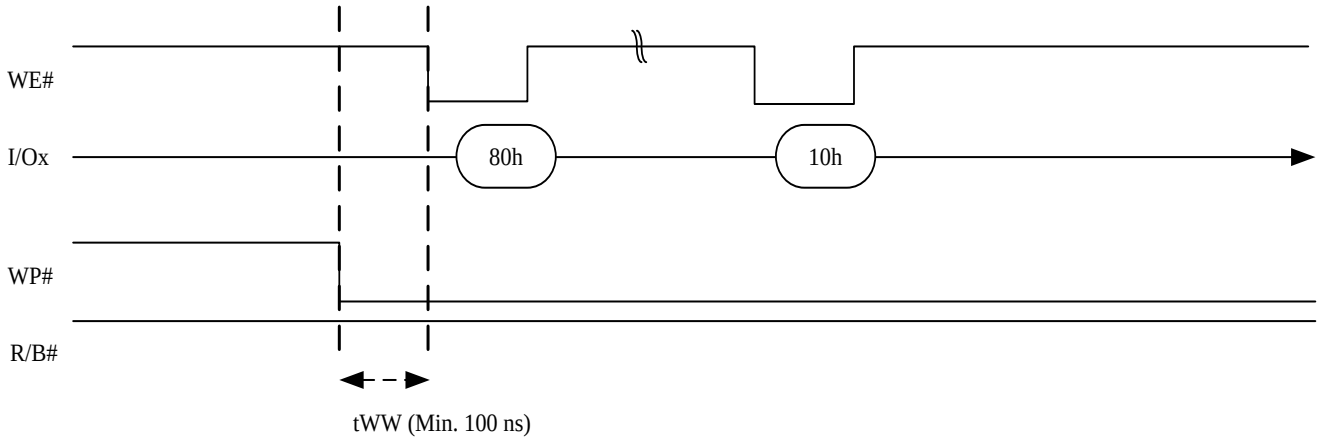
Enable Programming



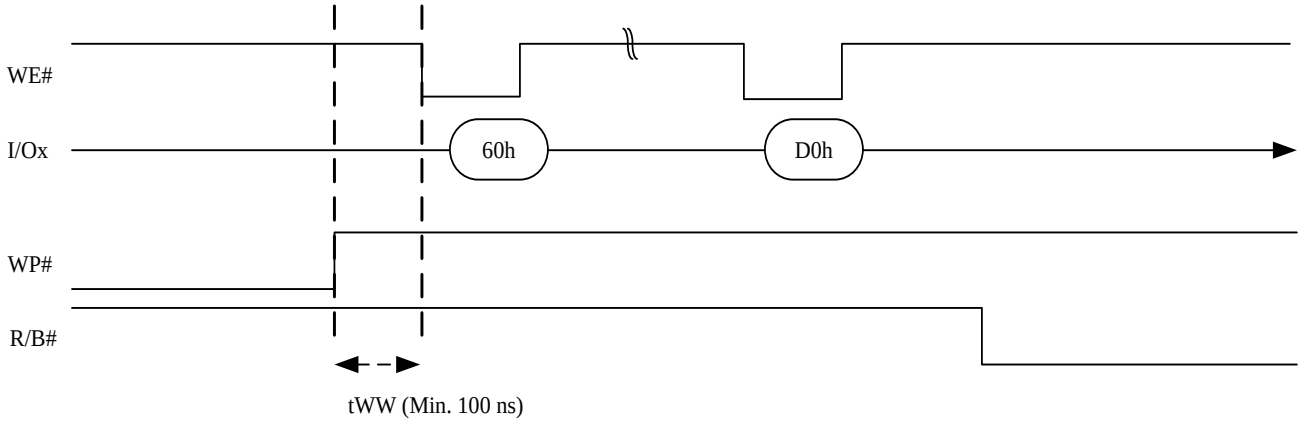
tWW (Min. 100 ns)

NOTE: WP# keeps "High" until programming finish.

Disable Programming



Enable Erasing



NOTE: WP# keeps “High” until erasing finish.

Disable Erasing

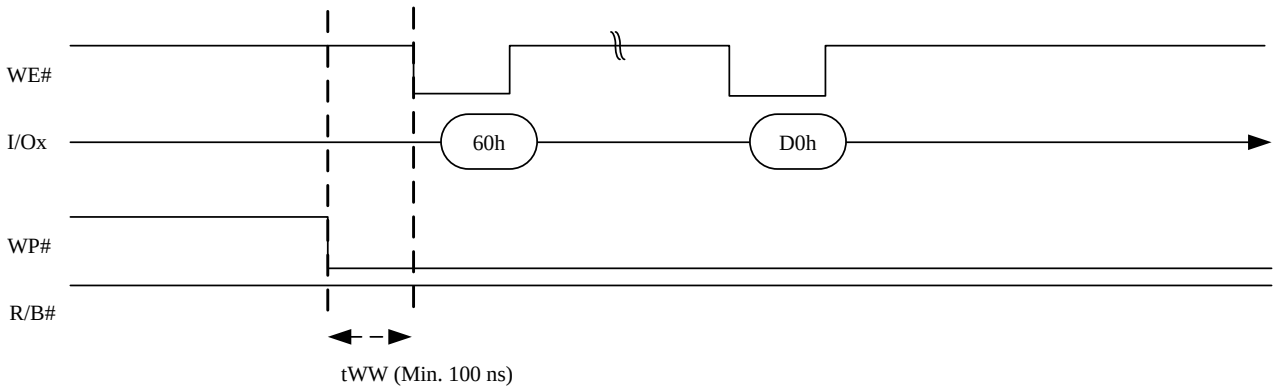


Figure Erase and Program Operations

BLOCK LOCK Operation

The block lock feature protects either the entire device ranges of blocks from being programmed and erased. Using the block lock feature is preferable to using WP# to prevent PRORAM and ERASE operations. Contact to ESMT for using this feature.

Read Parameter Page Operation

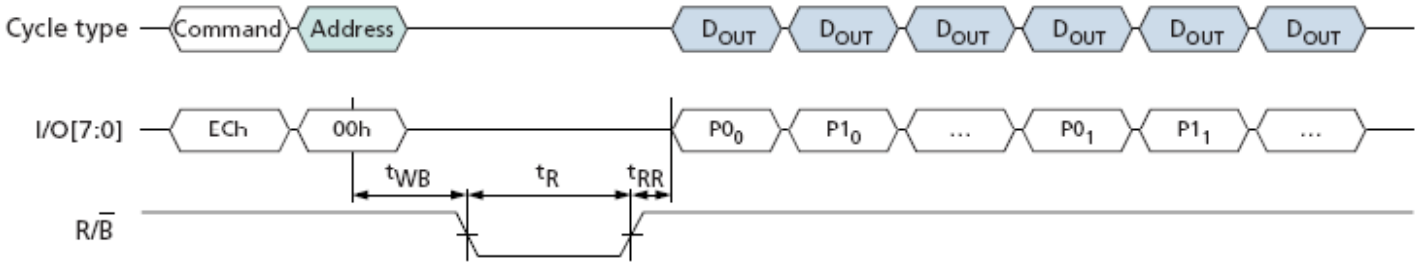
Read Parameter Page (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when the die(s) on the target is idle. Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When ECh command is followed by one 00h address cycle, the target goes busy for t_R. If the Read Status (70h) command is used to monitor for command completion, the Read mode (00h) command must be used to re-enable data output mode.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. Random Data Output (05h-E0h) can be used to change the location of data output.

The upper eight I/Os on a X16 device are not used and are a “Don’t care” for X16 devices.

Read Parameter Page Operation



Parameter Page Data Structure Table

Byte	Description		Value
0-3	Parameter page signature ("O", "N", "F", "I")		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	F59D1G81MB	10h, 00h
		F59D1G161MB	11h, 00h
8-9	Optional commands supported		33h, 00h
10~31	Reserved		All 00h
32-43	Device manufacturer		50h, 4Fh, 57h, 45h, 52h, 43h, 48h, 49h, 50h, 20h, 20h, 20h
44-63	Device model	F59D1G81MB	50h, 53h, 52h, 31h, 47h, 41h, 33h, 30h, 44h, 54h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		F59D1G161MB	50h, 53h, 52h, 31h, 47h, 41h, 34h, 30h, 44h, 54h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C8h
65-66	Date code		00h, 00h
67-79	Reserved		All 00h
80-83	Number of data bytes per page		00h, 08h, 00h, 00h
84-85	Number of spare bytes per page		40h, 00h
86-89	Number of data bytes per partial page		00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page		10h, 00h
92-95	Number of pages per block		40h, 00h, 00h, 00h
96-99	Number of blocks per unit		00h, 04h, 00h, 00h
100	Number of logical units		01h
101	Number of address cycles		22h
102	Number of bits per cell		01h
103-104	Number of maximum bad blocks per unit		14h, 00h
105-106	Block endurance		01h, 05h
107	Guaranteed valid blocks at beginning of target		01h
108-109	Block endurance of guaranteed valid blocks		00h, 00h
110	Number of partial programs per page		04h
111	Partial programming attributes		00h
112	Number of bits ECC		04h
113	Number of Interleaved address bits		00h
114	Interleaved operation attributes		00h
115-127	Reserved		All 00h
128	I/O pin capacitance		0Ah
129-130	Timing mode support (Reserved)		03h, 00h
131-132	Program cache timing mode support (Reserved)		03h, 00h
133-134	tPROG (max)		EEh, 02h
135-136	tBERS (max)		10h, 27h
137-138	tR (max)		19h, 00h
139-140	tCCS (min)		64h, 00h
141-163	Reserved		All 00h
164-165	Vendor-specific revision number		01h, 00h
166	Two-Plane Page Read support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support Two Plane Page Read		00h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support ONFI-specific read cache		00h

Byte	Description	Value
168	Read Unique ID support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support ONFI-specific Read Unique ID	00h
169	Programmable output impedance support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support programmable output impedance support	00h
170	Number of programmable output impedance support settings Bit[7:3]: Reserved (0) Bit[2:0]: Number of programmable IO output impedance settings	00h
171	Reserved	00h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support programmable R/B# pull-down strength	00h
173	Reserved	00h
174	Number of programmable R/B# pull-down strength support Bit[7:3]: Reserved (0) Bit[2:0]: Number of programmable R/B# pull-down strength settings	00h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 0= Doesn't support Get/Set Feature command set Bit 0: 1= support OTP mode	01h
176	OTP page start Bit[7:0] = Page where OTP page space begins	00h
177	OTP Data Protect address Bit[7:0] = Page address to use when issuing OTP Data Protect command	00h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	~~1Eh~~ 1Ch
179	OTP Feature Address	90h
180-253	Reserved	All 00h
254-255	Integrity CRC	Set at test
256-511	Values of bytes 0-255	Values of bytes 0-255
512-767	Values of bytes 0-255	Values of bytes 0-255
768+	Additional redundant parameter pages	

Read Unique ID Operation

Read Unique ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when the die(s) on the target is idle. Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When EDh command is followed by one 00h address cycle, the target goes busy for t_R. If the Read Status (70h) command is used to monitor for command completion, the Read mode (00h) command must be used to re-enable data output mode. After t_R completes, the host enables data output mode to read the unique ID.

Sixteen copies of the unique ID data are store in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique ID data, and the second 16 bytes are the complement of the first 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. Random Data Output (05h-E0h) can be used to change the location of data output.

The upper eight I/Os on a X16 device are not used and are a “Don’t care” for X16 devices.

Read Unique ID Operation

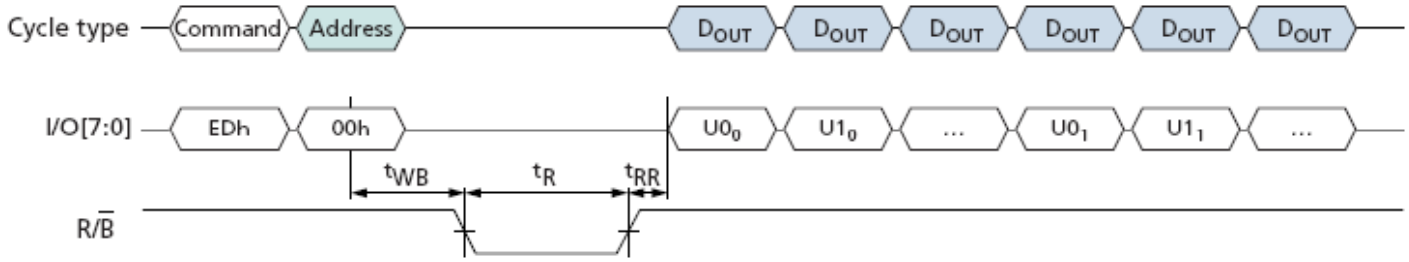


Figure Read Unique ID Operation

One-Time Programmable (OTP) Operations

This flash device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the Set Feature (EFh-90h-01h) command. When the device is in OTP operation mode, subsequent Read and/or Page Program are applied to the OTP area. **When you want to come back to normal operation, you need to use EFh-90h-00h for OTP mode release. Otherwise, device will stay in OTP mode.**

To program an OTP page, issue the Serial Data Input (80h) command followed by address cycles. The number of address cycles depends on the memory density; 4-byte address input is needed for 512Mb or 1Gb product, while 5-byte address input is needed for 2Gb or 4Gb product. The first two address cycles are column address that must be set as 00h. For the third cycle, select a page in the range of 00h through 1Dh. The fourth and fifth cycle is fixed at 00h. Next, up to 2,112 bytes of data can be loaded into data register. The bytes other than those to be programmed do not need to be loaded. Random Data Input (85h) command in this device is prohibited. The Page Program confirm (10h) command initiates the programming process. The internal control logic automatically executes the programming algorithm, timing and verification. Please note that **no partial-page program** is allowed in the OTP area. In addition, the OTP pages must be programmed in the ascending order. A programmed OTP page will be **automatically protected**.

Similarly, to read data from an OTP page, set the device to OTP operation mode and then issue the Read (00h-30h) command. The first two address cycles are column address that must be set as 00h and Random Data Output (05h-E0h) command is prohibited as well.

All pages in the OTP area will be protected simultaneously by issuing the Set Feature (EFh-90h-03h) command to set the device to OTP protection mode. After the OTP area is protected, no page in the area is programmable and the whole area cannot be unprotected.

The Read Status (70h) command is the only valid command for reading status in OTP operation mode.

OTP Modes and Commands

		Set feature	Command
OTP Operation mode	Read	EFh-90h[1]-01h[2]	00h-30h
	Page Program	EFh-90h-01h	80h-10h
OTP Protection mode	Program Protect	EFh-90h-03h	80h-10h
OTP Release mode	Leave OTP mode	EFh-90h-00h	-

NOTE:

1. 90h is OTP status register address.
2. 00h, 01h and 03h are OTP status register data values.

Description	Value
Number of OTP pages	30
OTP page address	00h – 1Bh
Number of partial page programs for each page in the OTP area	1

NOTE:

1. OTP page address 1Ch and 1Dh are also able to access, however, they both are read only for test mark.

Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

Read Status command 70h is used to retrieve operating status of commands like page read, page program and block erase. Similarly, Read Status Two-Plane Command F1h is used to retrieve operating status of two-plane commands. The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycle.

I/O	Page Program	Block Erase	Read	Cache Read	Definition
I/O 0	Pass/Fail	Pass/Fail	NA	NA	Pass : 0 Fail : 1
I/O 1	NA	NA	NA	NA	Don't cared
I/O 2	Pass/Fail (for OTP)	NA	NA	NA	Don't cared
I/O 3	NA	NA	NA	NA	Don't cared
I/O 4	NA	NA	NA	NA	Don't cared
I/O 5	NA	NA	NA	True Read/Busy	Busy : 0 Ready : 1
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Read/Busy	Busy : 0 Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected :0 Not Protected : 1

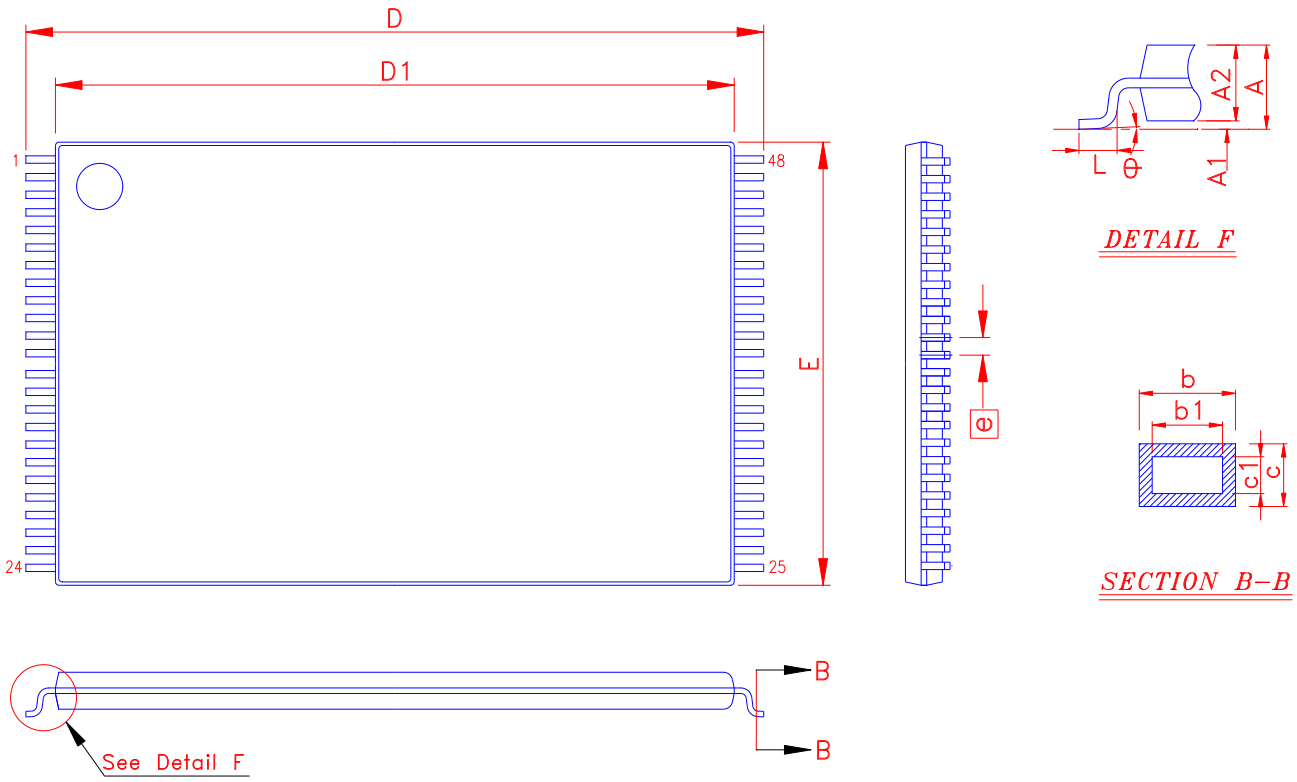
Table 3 Status Register Definition for 70h Command

NOTE :

1. I/Os defined 'NA ' are recommended to be masked out when Read Status is being executed.
2. n: current page, (n-1): previous page

PACKING DIMENSION

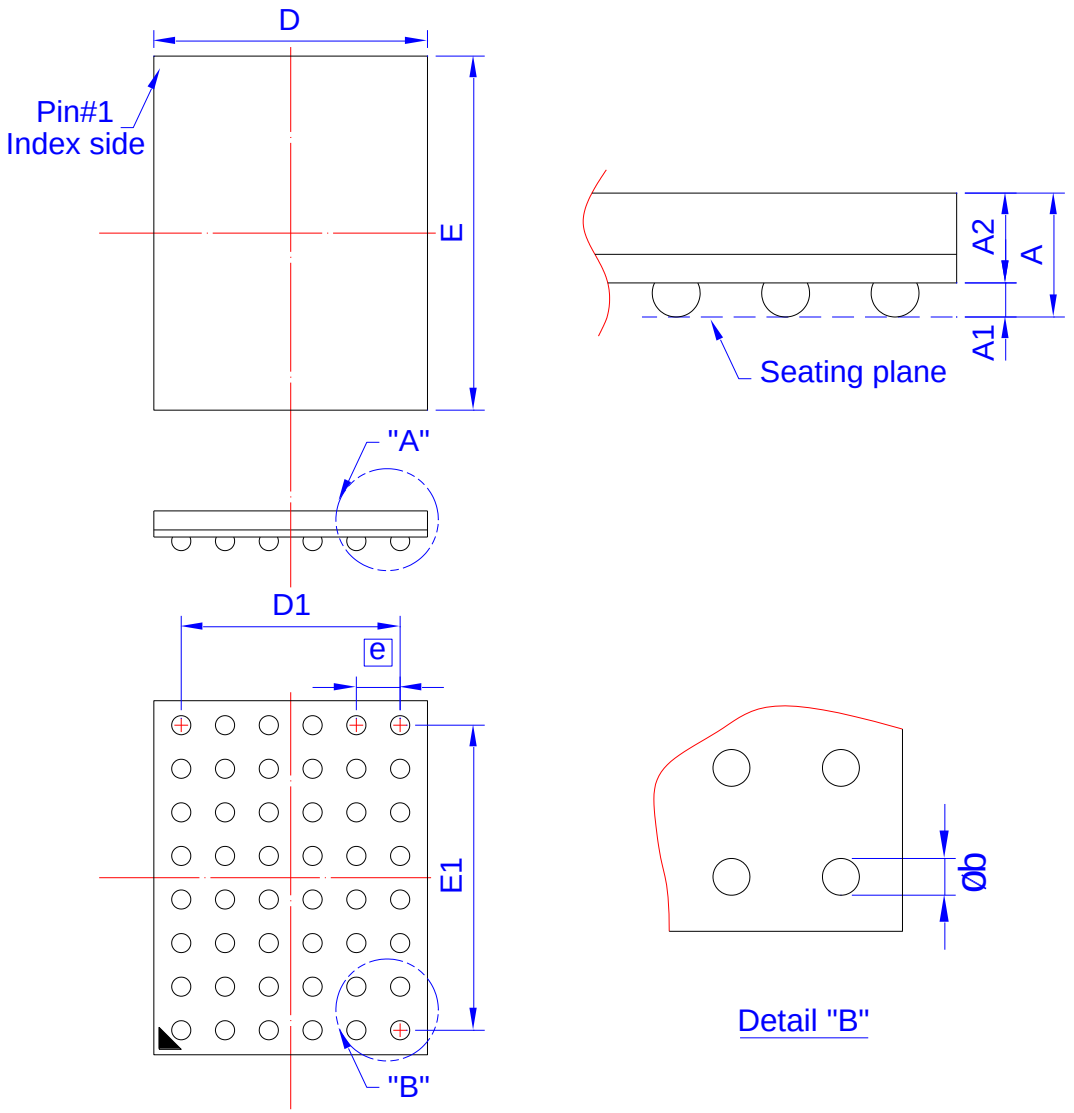
48-LEAD TSOP(I) (12x20 mm)



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	-------	-------	1.20	-------	-------	0.047	D	20.00 BSC			0.787 BSC		
A 1	0.05	-------	0.15	0.006	-------	0.002	D 1	18.40 BSC			0.724 BSC		
A 2	0.95	1.00	1.05	0.037	0.039	0.041	E	12.00 BSC			0.472 BSC		
b	0.17	0.22	0.27	0.007	0.009	0.011	e	0.50 BSC			0.020 BSC		
b1	0.17	0.20	0.23	0.007	0.008	0.009	L	0.50	0.60	0.70	0.020	0.024	0.028
c	0.10	-------	0.21	0.004	-------	0.008	θ	0^o	-------	8^o	0^o	-------	8^o
c1	0.10	-------	0.16	0.004	-------	0.006							

PACKING **DIMENSIONS**

48-BALL **Flash (6.5x5 mm)**

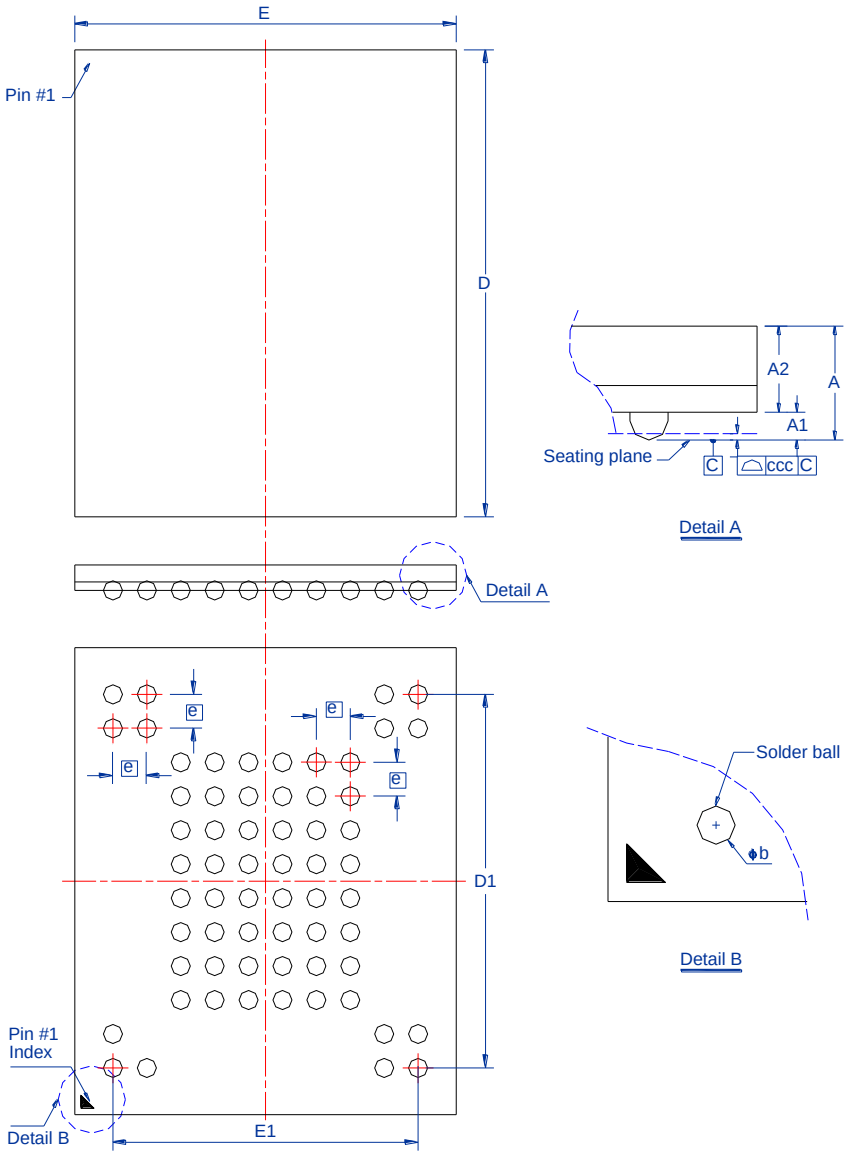


Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			0.80			0.031
A_1	0.22	0.27	0.32	0.009	0.011	0.013
A_2		0.48			0.019	
Φ_b	0.30	0.35	0.40	0.012	0.014	0.016
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.40	6.50	6.60	0.252	0.256	0.260
D_1	4.00 BSC			0.157 BSC		
E_1	5.60 BSC			0.220 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.
(Revision date : Apr 10 2018)

PACKING DIMENSIONS

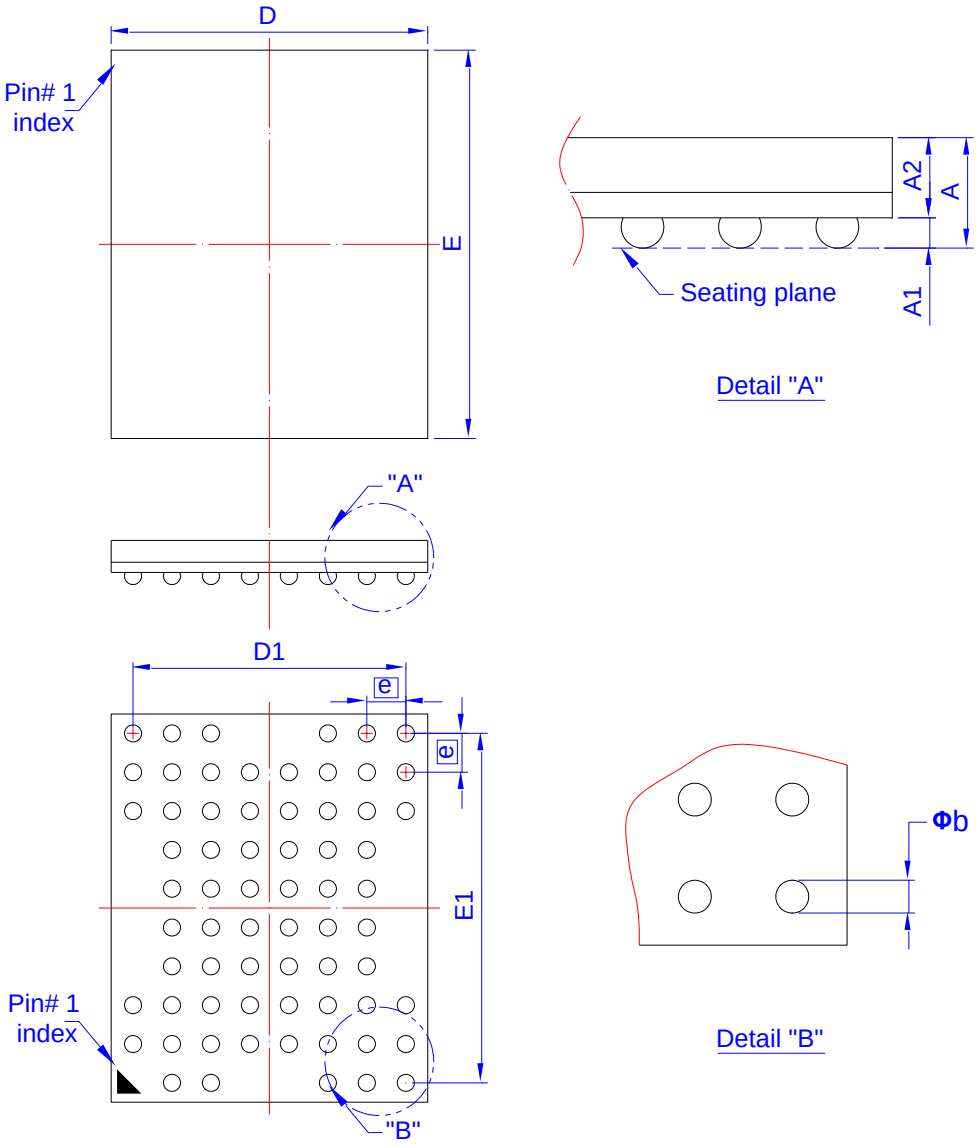
63-BALL 1G NAND Flash (9x11 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			1.00			0.039
A_1	0.25		0.35	0.010		0.014
A_2		0.60 BSC			0.024 BSC	
Φb	0.40		0.50	0.016		0.020
D	10.90	11.00	11.10	0.429	0.433	0.437
E	8.90	9.00	9.10	0.350	0.354	0.358
D_1		8.80 BSC			0.346 BSC	
E_1		7.20 BSC			0.283 BSC	
e		0.8 BSC			0.031 BSC	
ccc			0.10			0.004

Controlling dimension : Millimeter.

PACKING DIMENSIONS
67-BALL Flash (6.5x8 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			1.00			0.039
A_1	0.22	0.27	0.32	0.009	0.011	0.013
A_2	0.61	0.66	0.71	0.024	0.026	0.028
Φ_b	0.30	0.35	0.40	0.012	0.014	0.016
D	6.40	6.50	6.60	0.252	0.256	0.260
E	7.90	8.00	8.10	0.311	0.315	0.319
D_1	5.60 BSC			0.220 BSC		
E_1	7.20 BSC			0.283 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.
(Revision date : Jun 29 2014)

Revision History

Revision	Date	Description
0.1	2017.06.20	Original
0.2	2017.08.21	Modify BLOCK LOCK Operation description
0.3	2018.04.13	Add 48 ball BGA packing
1.0	2018.08.14	1. Delete Preliminary 2. Correct typo
1.1	2019.01.07	Add 48 ball WLCSP package
1.2	2025.04.07	Modify: 48 ball WLCSP package removed

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